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A STUDY OF TWO CONTROL METHODS FOR FULL BRIDGE CONVERTERS: SOFT SWITCH BYPASS AND CURRENT MODE CONTROL

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In a broad sense, there are now 3 basic catagories for high power (above several KW) DC/DC converters: 1) Forced commutation (FC) 2) Resonant (R) 3) Soft switch (SS). Some topologies that are combinations of the above also have been proposed, such as certain pulse width modulation (PWM)-resonant arrangements. The first part of this project was a proposed improvement of the third catagory, the soft switch. The basic idea of this new converter was to use two additional switches that would bypass the load during part of the operating cycle if the current decreased below a certain level. The motivation for this was to retain the soft switching characteristic at light loads--a common problem with previous soft switch converters.

Although the bypass circuit proved functional, certain problems were uncovered which raise doubts about its ultimate feasibility. Because of these problems, the research emphasis was shifted from the bypass to an improved current mode control (CMC) converter that promised better results.

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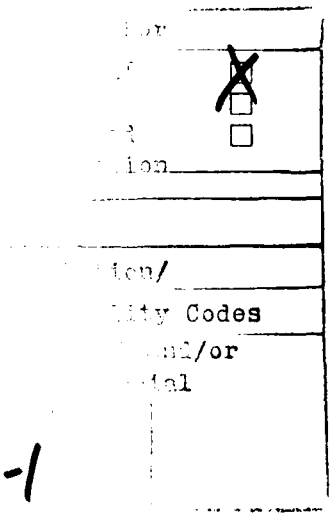
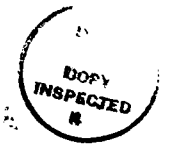
FOREWORD

This report presents the results of research performed under work order SCEE-SRAP/89-0023 which was performed by The University of Toledo for the Wright Research and Development Center, Aeropropulsion and Power Laboratory over the period May 1, 1989 to March 11, 1990. These subcontracts were administeed by the Southeastern Center for Electrical Engineering Education, St. Cloud, Florida.





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I. INTRODUCTION

1.1 Background

In a broad sense, there are now three basic categories for high power (above several KW) DC/DC converters:

1. Forced commutation (FC)
2. Resonant (R)
3. Soft switch (SS).

Some topologies that are combinations of the above also have been proposed, such as certain pulse width modulation (PWM)-resonant arrangements. The first part of this project was a proposed improvement of the third category, the soft switch. The basic idea of this new converter was to use two additional switches that would bypass the load during part of the operating cycle if the current decreased below a certain level. The motivation for this was to retain the soft switching characteristic at light loads - a common problem with previous soft switch converters.

Although the bypass circuit proved functional, certain problems were uncovered which raise doubts about its ultimate feasibility. Because of these problems, the research emphasis was shifted from the bypass to an improved current mode control (CMC) converter that promised better results.

1.2 Previous Research

To explain the interest in soft switching methods, it is useful to briefly review some of the characteristics of the three converter types listed in the previous section.

1.2 .1 Forced Commutation

A basic full bridge version of this circuit is shown in Fig. 1.1. The circuit

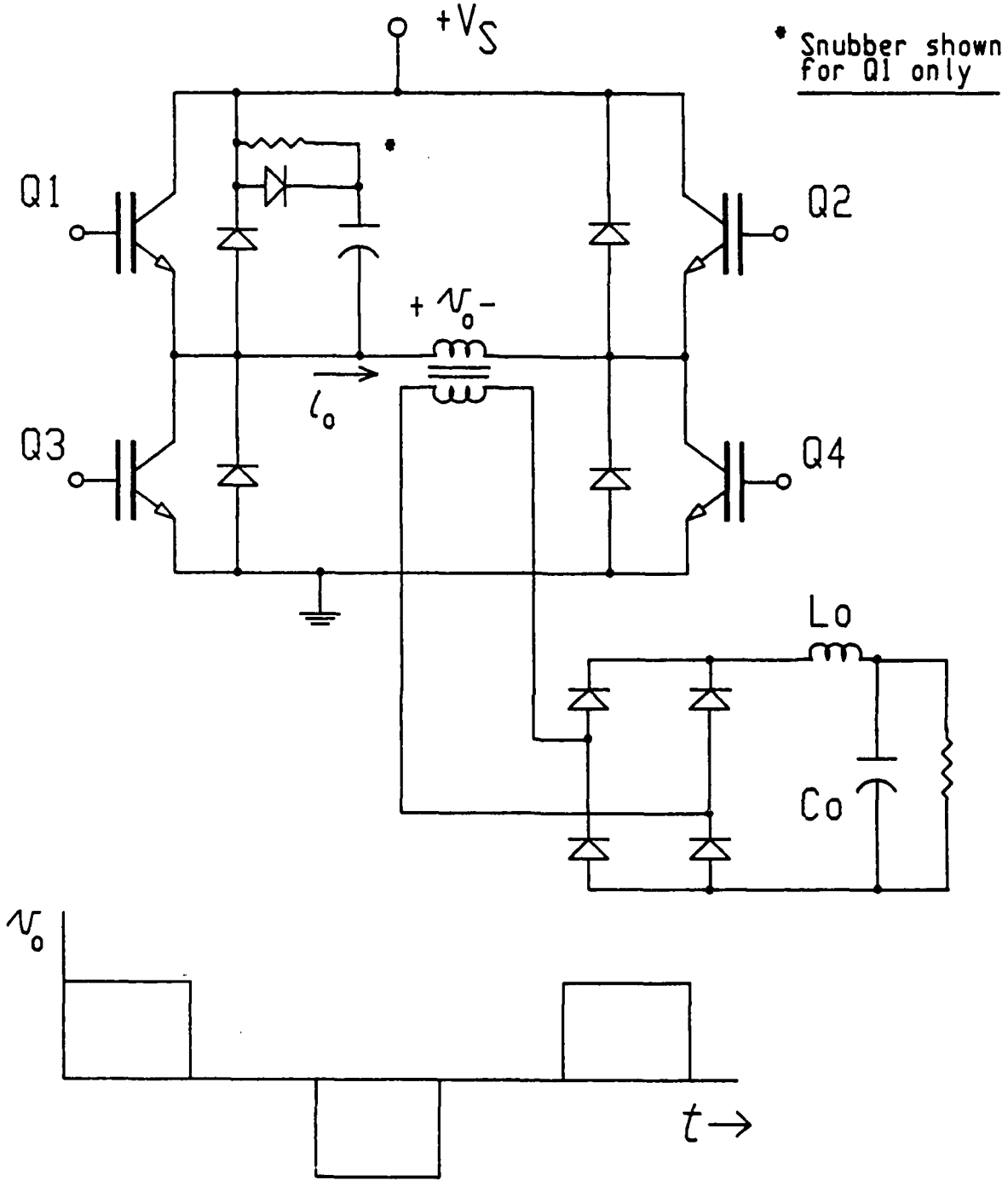


Fig. 1.1. Full bridge PWM converter.

operates at constant frequency, and the output voltage is controlled by varying its duty cycle. Current mode control (CMC) [2-4] provides symmetry for the output waveforms and thus avoids transformer saturation. The obvious disadvantage of the circuit is the higher switching loss and EMI that result from forced commutation. This loss is rapidly decreasing however, as faster switching devices are now becoming available.

1.2.2 Resonant

A full bridge version of the series resonant converter (SRC) is shown in Fig. 1.2 [5-8]. Numerous varieties of other resonant circuits also have been proposed, but the basic SRC is probably still the best topology for high power applications. In any case, some of its pros and cons are similar to other resonant circuits, so it is used as an example. As seen from the current waveform, the switches naturally commutate at zero current, which implies almost no turn-off loss. The switches do exhibit some turn-on loss since this current transition is abrupt, but this is generally small because of the relatively fast turn-on time. The diodes, D1-D4, also have some turn-off loss since they are force commutated. Since the resonant frequency of the i_0 waveform is fixed, the output must be controlled by variation of the switching frequency. The circuit is very efficient because of the low switching loss, but the variable switching frequency is a distinct disadvantage. In particular, this doubles the size of the output transformer, and complicates the EMI filtering for nearby equipment.

1.2.3 Soft Switch

One version of this topology is shown in Fig. 1.3. [1]. This circuit is similar to the FC circuit in Fig. 1.1, except that L_0 is now in series with the transformer

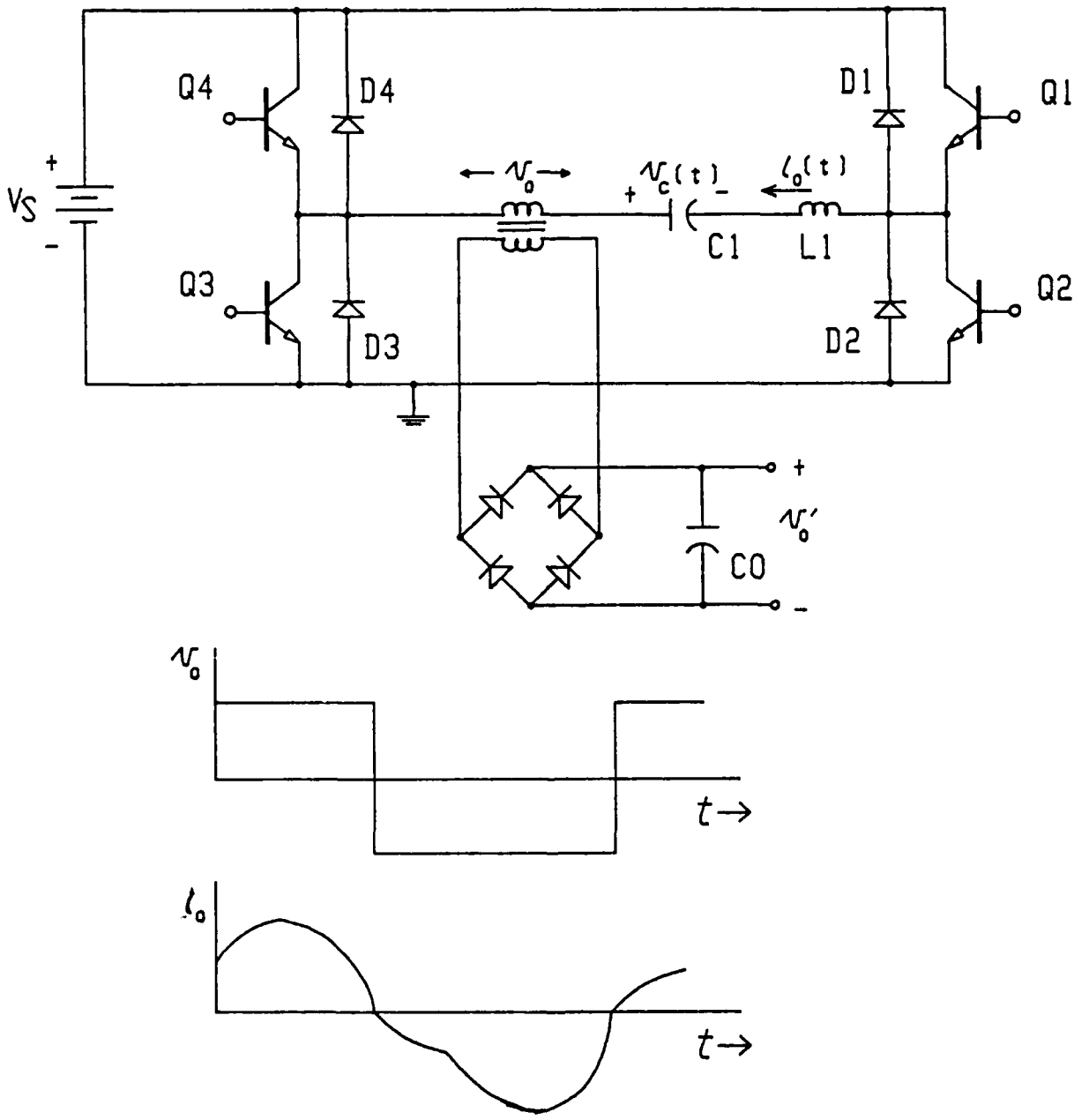


Fig. 1.2. Full bridge series resonant converter.

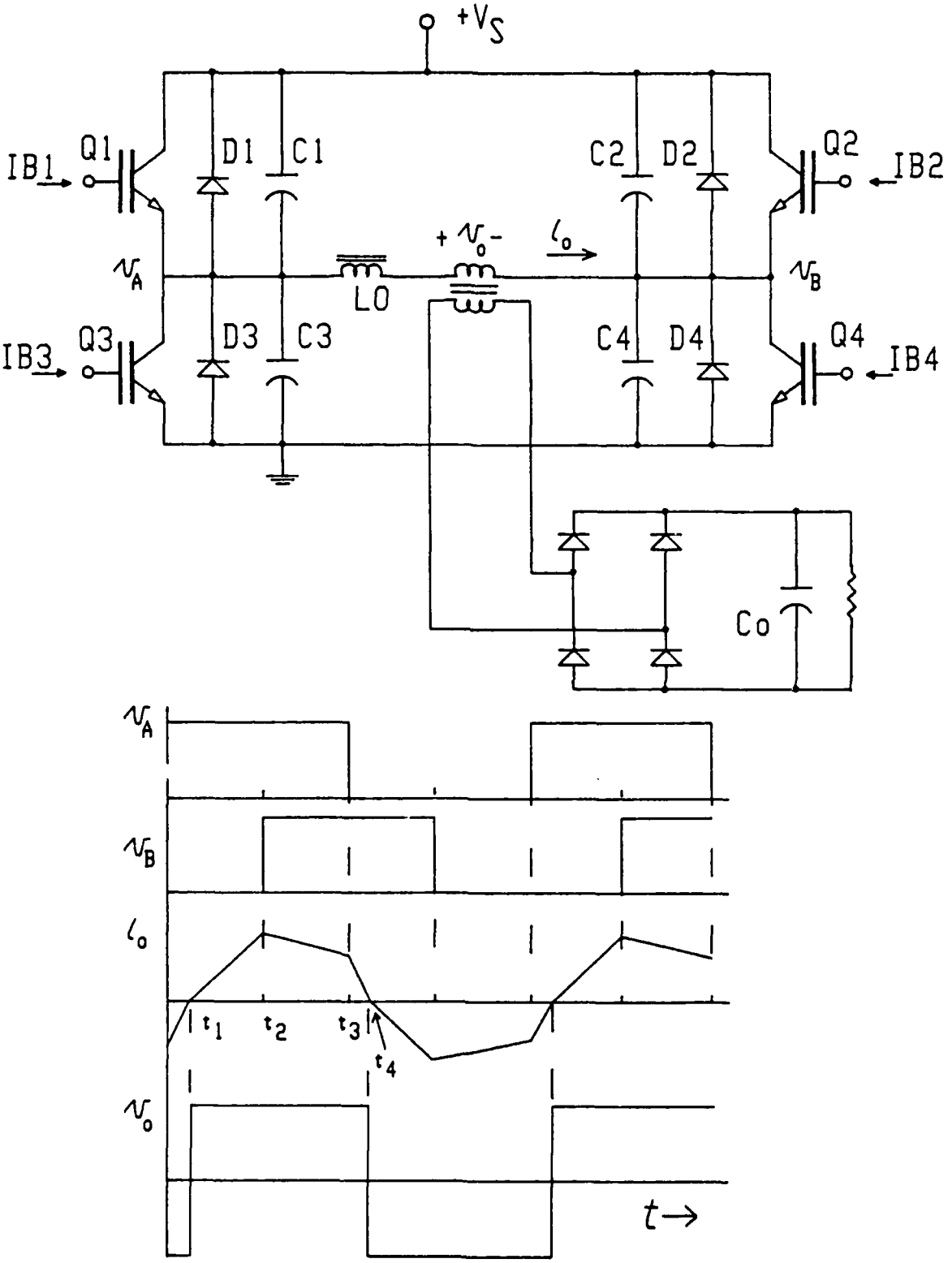


Fig. 1.3. Full bridge soft switch converter.

primary, and the RDC snubbers are replaced by C1-4. Soft switching is a relatively new technique that provides both constant frequency operation and very low switching loss at loads above about 50% of full load. The traditional problem has been that soft switching doesn't occur at small loads.

In Fig. 1.3 Q1 and Q4 are on together until Q4 is switched off at t_2. Although the very small charging times of C1-4 are not shown, at t_2 C4 will rapidly charge to V_s and C2 will discharge to 0, at which time D2 conducts. Note that Q4 has almost no turn off loss because C4 essentially clamps the Q4 voltage to zero during turn-off. Q1 and D2 conduct until Q1 is turned off at t_3. C1 then rapidly charges to V_s while C3 simultaneously discharges to 0. D3 and D2 then conduct until $i_0 = 0$ at t_4. Q2 and Q3 then turn on to start the next half cycle. Note that Q1-4 turn-off at zero voltage and turn-on into zero current. This reduces both turn-off and turn-on losses at almost zero. *Likewise D1-4 turn-off at zero current which reduces* their turn-off losses to almost zero.

The problem with this circuit is that the desired mode of operation requires continuous current, which only occurs at fairly heavy loads. Suppose Q4 is turned off with a small load at t_2 as shown in Fig. 1.4. In this case the $\frac{1}{2} i_0^2(t_2) L_o$ energy stored in L_0 at turn-off is too small to keep Q1 and D2 in conduction until Q3 is turned on at t_3. The sequence that should occur at t_3 is:

1. Q1 turns off.
2. C1 charges to V_s and C3 discharges to 0.
3. D3 conducts until $i_o = 0$.
4. Q3 turns on.

Instead, C3 will remain charged close to V_s until Q3 turns on at t_3. The resulting

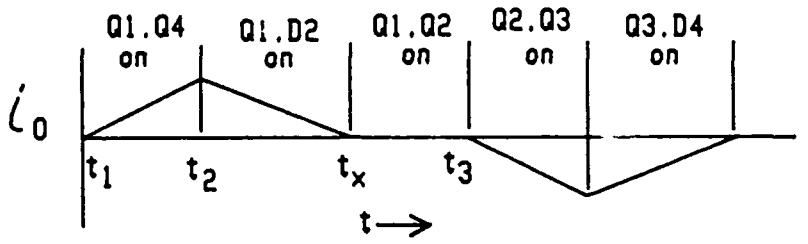


Fig. 1.4. Conventional soft switch converter current at light load.

high discharge current through Q3 and charging current through C1 will produce high turn on losses which may even destroy the switch. Reference [1] indicates that this commutation problem will typically occur at any load below about 50% of full load for the version in Fig. 1.3. This reference also proposes a more complex version using two full bridge circuits. This dual converter will operate over a wider load range, but commutation problems will still occur at significant loads if there is any variation in V_s (this is also shown in [1].)

1.3 Soft Switch with Bypass

Because of commutation failures at smaller loads, the soft switch converter is presently restricted to applications with rather limited variations in load and V_s . As stated earlier, the basic problem is that the 1/2 i_o^2 L_o energy is not high enough to insure a continuous i_o at smaller loads.

In an effort to solve this commutation problem, a circuit similar to the bypass converter in Fig. 1.5 was investigated. Note that Fig. 1.5 is the same as Fig. 1.3 except that the instantaneous value of i_o is monitored by the CT and bypass switches Q5 and Q6 are connected in parallel with the output rectifier bridge. By monitoring i_o, the controller can determine if 1/2 i_o^2 L_o is large enough to maintain continuous conduction.

A typical half cycle of operation proceeds in the following manner. Assume Q1 and Q4 are on, and the time comes to turn off Q4. If the monitored i_o is above a certain level, I_{x1}, Q4 is turned off, but Q5 is turned on. If i_o is below I_{x1}, Q5 is still turned on, but Q4 is not turned off until i_o reaches I_{x1}. This allows 1/2 i_o^2 L_o to reach an adequate level to provide proper commutation. Q4 is now off, and the charging of C4 and discharging of C2 occurs rapidly. L_o is now shorted

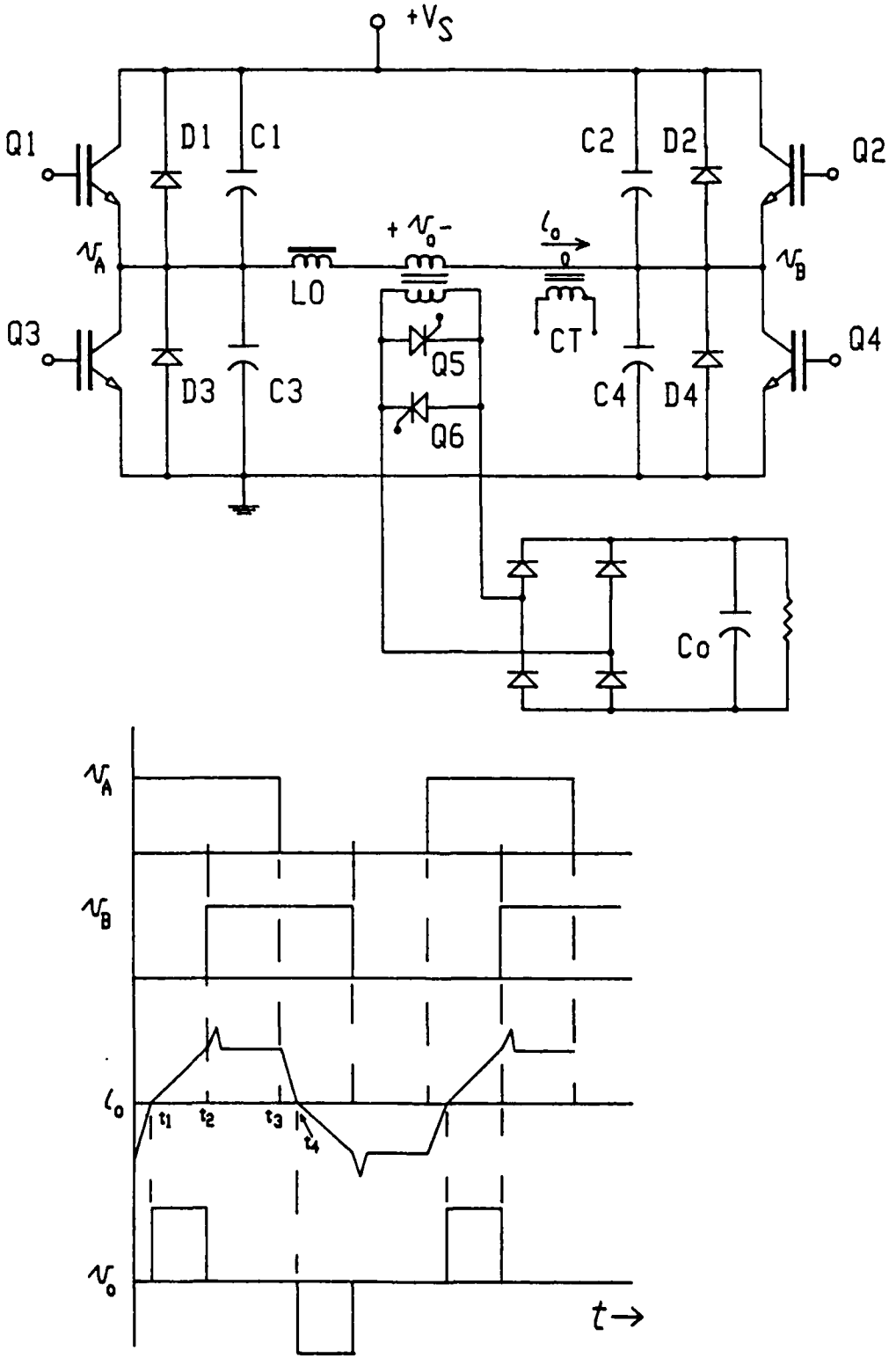


Fig. 1.5. Full bridge bypass converter.

by Q1, Q5 and D2. When Q1 turns off, i_o should be at an adequate level to discharge C3 and charge C1, and the remaining 1/2 i_o^2 L_o energy is dumped into V_s via D2 and D3. When i_o reaches zero, Q2 and Q3 begin to conduct, reversing i_o for the start of the next half cycle. As mentioned previously, a small version of this circuit was built and tested at a power level of 180 watts. The circuit proved to be functional, but the following problems were discovered:

1. The control circuit is very complex
2. The converter exhibits a randomly occurring mode where the conduction intervals for the two half cycles become highly unbalanced.
3. The circuit does not appear to be any more efficient than conventional PWM.

Because of these problems, the development of this converter was discontinued, and the research was focused on the full bridge CMC converter.

1.4 Full Bridge CMC

In light of the problems with soft switch and resonant converters, a force commutated converter with CMC may well be the optimum choice at higher power levels. This possibility seems all the more reasonable because of the relatively low switching loss of the newer FETs and IGTs, and it may be even more likely with the new MCT device.

However, it is generally accepted that the full bridge topology is the optimum choice for higher power levels, and the technical literature on full bridge CMC is surprisingly sparse [9]. Because of the possible benefits of such a circuit and the apparent lack of published results, it was decided to build and test a 1 kW version to study its feasibility.

II. STEADY STATE ANALYSIS OF THE SOFT SWITCH CONVERTER

2.1 Continuous Current Operation Without Bypass

The circuit for the full bridge soft switch converter without the bypass is shown in Fig. 1.3 while the detailed i_o waveform is shown in Fig. 2.1. The output voltage is regulated by phase shift control, where all switches operate at a duty cycle of almost 50%. Regulation is achieved by variation of the phase shift between v_a and v_b. If the load current is high enough, soft switching will occur as described in the previous section. A typical cycle for this case can be analyzed by means of the proper equivalent circuits and detailed i_o waveform in Fig. 2.1

$0 \le t \le t_o$: Q1, Q4 = on

$$\therefore I_{oo} = \frac{(V_s - V_o)\, t_o}{L} \tag{2.1}$$

(2.1) can be re-written, $\Delta t_o = t_o = \dfrac{L I_{oo}}{(V_s - V_o)}$ (2.2)

$t_o < t < t_1$: Q1 = on, C4 charges, C2 discharges

The equivalent circuit is shown in Fig. 2.2

For the i_2 loop,

$$\frac{V_s}{s} = I_1 Ls + I_2 \left(Ls + \frac{1}{Cs}\right) - I_{oo}L + \frac{V_o}{s} \tag{2.3}$$

For the i_1 loop,

$$\frac{V_s}{s} = I_2 Ls + I_1 \left(Ls + \frac{1}{Cs}\right) - I_{oo}L + \frac{V_o}{s} \tag{2.4}$$

Comparison of (2.3) and (2.4) indicates that

$$I_1 = I_2 \tag{2.5}$$

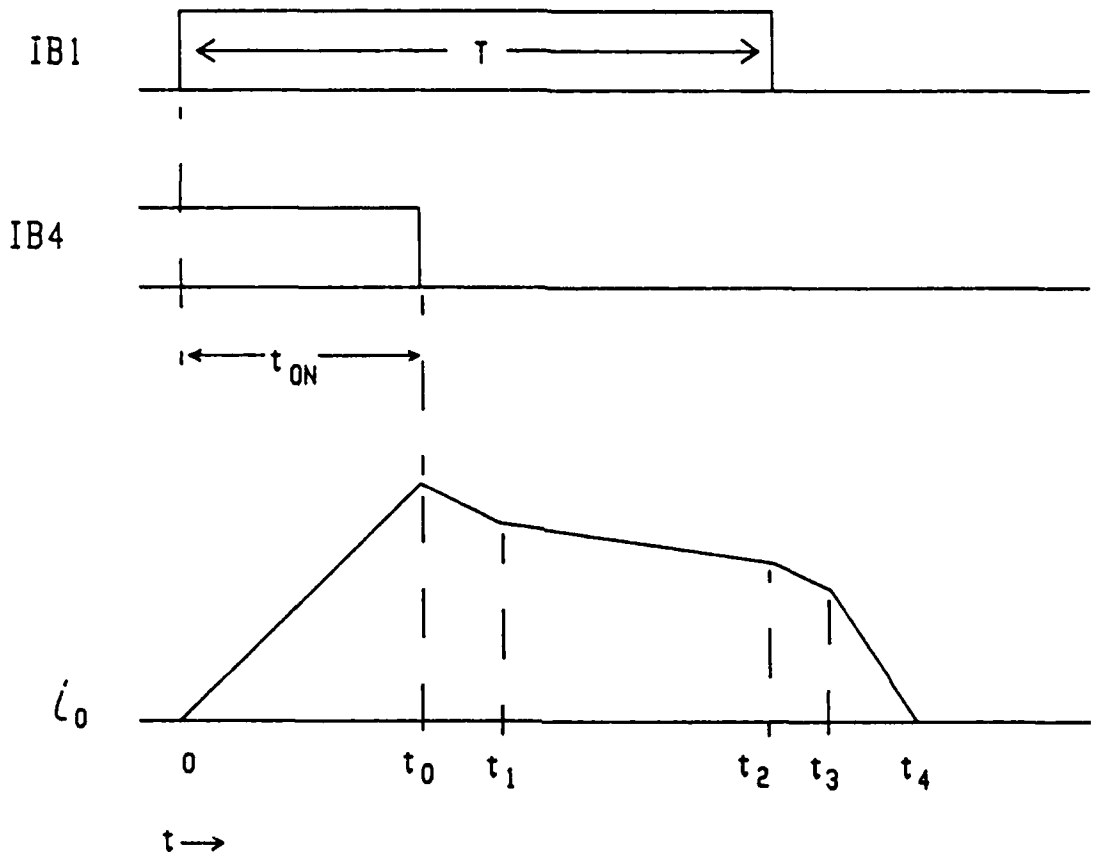
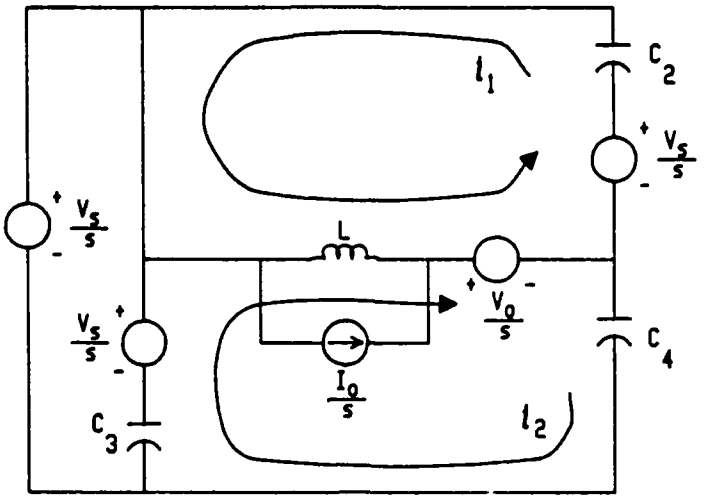


Fig. 2.1. i_o without bypass.



$C_i = c.\ i=1-4$

Fig. 2.2. Equlvalent circuit for $t_0 \leq t \leq t_1$.

$$\therefore I_1\left(2Ls + \frac{1}{Cs}\right) = \frac{V_s - V_o}{s} + I_{oo}L \tag{2.6}$$

$$I_1 = \frac{V_s - V_o}{2L\left(s^2 + \frac{1}{2LC}\right)} + \frac{I_{oo}s}{2\left(s^2 + \frac{1}{2LC}\right)} \tag{2.7}$$

$$\therefore i_1(t) = i_2(t) = \frac{V_s - V_o}{\sqrt{\frac{2L}{C}}} \sin(w_1 t) + \frac{I_{oo}}{2}\cos(w_1 t) \tag{2.8}$$

$$\text{where } w_1 = \frac{1}{\sqrt{2LC}}, \tag{2.9}$$

$$\therefore i_{L1} = i_1(t) + i_2(t) = \frac{2(V_s - V_o)}{\sqrt{\frac{2L}{C}}} \sin(w_1 t) + I_{oo}\sin(w_1 t + 90^\circ) \tag{2.10}$$

In phasor form,

$$I_{L1}\angle\theta_1 = \frac{2(V_s - V_o)}{\sqrt{\frac{2L}{C}}}\angle 0^\circ + I_{oo}\angle 90^\circ \tag{2.11}$$

as shown in Fig. 2.3.

$$\therefore I_{L1} = \left[\frac{2(V_s - V_o)^2 C}{L} + I_{oo}^2\right]^{1/2} \tag{2.12}$$

$$\theta_1 = \tan^{-1}\left(\frac{I_{oo}\sqrt{\frac{2L}{C}}}{2(V_s - V_o)}\right), \quad 0 \le \theta_1 \le 90^\circ \tag{2.13}$$

$$\text{and} \qquad i_{L1}(t) = I_{L1}\sin(w_1 t + \theta_1) \tag{2.14}$$

$$\text{if } \Delta t_1 = t_1 - t_o,$$

$$I_{01} = I_{L1}\sin[w_1(\Delta t_1) + \theta_1] \tag{2.15}$$

To find Δt_1 we note that $v_{c4(\Delta t_1)} = V_s$,

$$\therefore v_{C4} = \frac{1}{C}\int_o^t i_{2(t)}dt \tag{2.16}$$

$$v_{C4} = \frac{V_s - V_o}{\sqrt{2LC}}\left[-\frac{\cos w_1 t}{w_1}\right]_o^t + \frac{I_{oo}}{2C}\left[\frac{\sin w_1 t}{w_1}\right]_o^t \tag{2.17}$$

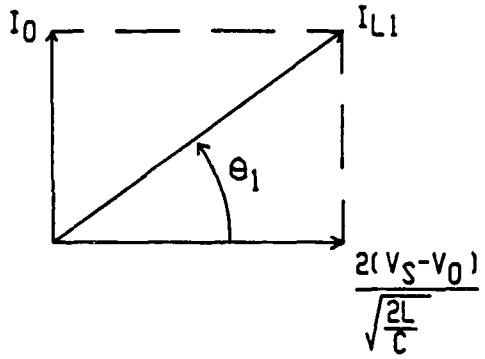


Fig. 2.3. Phasor diagram for $I_{L1}\angle\theta_1$.

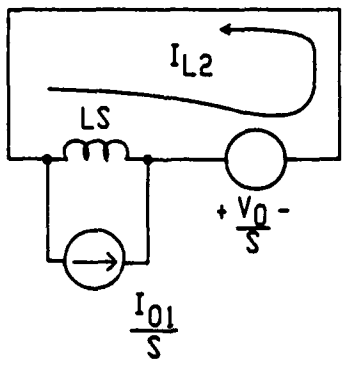


Fig. 2.4. Equivalent circuit for $t_1 \ll t \ll t_2$.

$$\therefore\ v_{C4} = (V_s - V_o)[1 - \cos(w_1 t)] + I_o\sqrt{\frac{L}{2C}}\sin(w_1 t) \tag{2.18}$$

$$\therefore\ v_{C4} = V_s - V_o + V_{C4}\sin(w_1 t + \theta_2) \tag{2.19}$$

$$\text{where } V_{C4} = \left[\frac{I_o^2 L}{2C} + (V_2 - V_o)^2\right]^{1/2} \tag{2.20}$$

$$\theta_2 = \tan^{-1}\left[\frac{-(V_s - V_o)}{I_o\sqrt{\frac{L}{2C}}}\right] \tag{2.21}$$

$$@\ v_{C4} = V_s\ ,\ V_{C4}\sin[w_1(\Delta t_1) + \theta_2] = V_o \tag{2.22}$$

$$\therefore\ \Delta t_1 = \sqrt{2LC}\left[\sin^{-1}\left(\frac{V_o}{V_{C4}}\right) - \theta_2\right] \tag{2.23}$$

$t_1 \le t \le t_2$: Q1, D2 = on

From Fig. 2.4,

$$i_{L2(t)} = I_{01} - \frac{V_o}{L}t\ ,\ t_1 \le t \le t_2 \tag{2.24}$$

$$\text{where } t = t - t_1 \tag{2.25}$$

$$\therefore\ I_{02} = I_{01} - \frac{V_o}{L}(\Delta t_2) \tag{2.26}$$

where $\Delta t_2 = t_2 - t_1$

$t_2 \le t \le t_3$: D2 = on , C1 charges, C3 discharges.

For the i_1 loop in Fig. 2.5,

$$I_1\left(Ls + \frac{1}{Cs}\right) - LI_{02} + \frac{V_o}{s} + I_2 Ls = 0 \tag{2.27}$$

For the i_2 loop,

$$I_2\left(Ls + \frac{1}{Cs}\right) - LI_{02} + \frac{V_o}{s} + I_1 Ls = 0 \tag{2.28}$$

Comparison of (2.27) and (2.28) indicates that

$$I_1 = I_2 \tag{2.29}$$

$$\therefore i_{1(t)} = \frac{-V_o}{\sqrt{\frac{2L}{C}}} \sin(w_1 t) + \frac{I_{02}}{2} \cos(w_1 t) \tag{2.30}$$

$$\text{define, } \Delta t_3 = t_3 - t_2 \tag{2.31}$$

Assuming the circuit works properly, it is necessary to find the value of $v_{C1}(t_3) = V_s$.

$$v_{C1(t)} = \frac{1}{C}\int_o^t i_{1(t)}dt = -V_o + V_o \cos w_1 t + \frac{I_{02}}{2}\sqrt{\frac{2L}{C}} \sin w_1 t$$

$$= -V_o + V_x \sin(w_1 t + \theta_2) \tag{2.32}$$

where $V_x = \left[V_o^2 + \frac{I_{02}^2 L}{2C}\right]^{1/2}$

$$\theta_2 = \tan^{-1}\left(\frac{2V_o}{I_{02}}\sqrt{\frac{C}{2L}}\right) \tag{2.33}$$

$$\therefore v_{C1}(\Delta t_3) = V_s = -V_o + V_x \sin(w\Delta t_3 + \theta_2) \tag{2.34}$$

$$\therefore \Delta t_3 = \sqrt{2LC}\left[\sin^{-1}\left(\frac{V_s + V_o}{V_x}\right) - \tan^{-1}\left(\frac{2V_o}{I_{02}}\sqrt{\frac{C}{2L}}\right)\right] \tag{2.35}$$

If the circuit doesn't work properly, $i_{1(t)}$ will decay to 0 at some Δt_x before v_{C1} reaches V_s. For this case, Δt_x can be found as follows,

$$i_{1(\Delta t_x)} = 0 = \frac{-V_o}{\sqrt{\frac{2L}{C}}} \sin(w_1 \Delta t_x) + \frac{I_{02}}{2} \cos(w_1 \Delta tx) \tag{2.36}$$

$$\therefore \Delta t_x = \frac{1}{w_1} \tan^{-1}\left(\frac{I_{02}}{2V_o}\sqrt{\frac{2L}{C}}\right) \tag{2.37}$$

For satisfactory operation, it is necessary that,

$$\Delta t_x > \Delta t_3 \tag{2.38}$$

Finally,

$$I_{03} = i_{1(\Delta t_3)} + i_{2(\Delta t_3)} = \frac{-2V_o}{\sqrt{\frac{2L}{C}}} \sin(w_1 \Delta t_3) + I_{02} \cos(w_1 \Delta t_3) \tag{2.39}$$

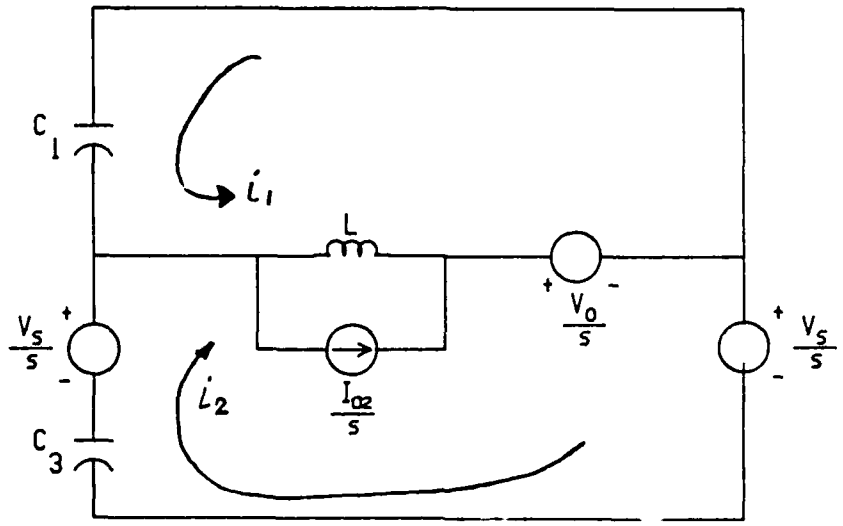


Fig. 2.5. Equlvalent circuit for $t_2 \leq t \leq t_3$.

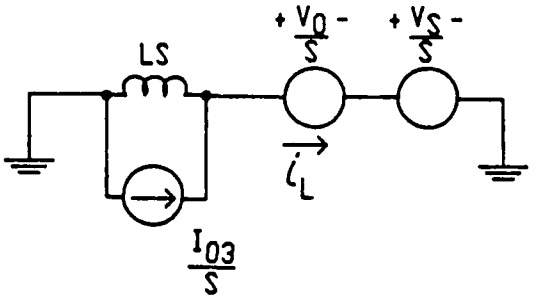


Fig. 2.6. Equivalent circuit for $t_3 \ll t \ll t_4$.

$t_3 \le t \le t_4$: D2, D3 = on, L energy is dumped into $V_o + V_s$.

From Fig. 2.6,

$$i_L(t) = I_{03} - \frac{V_o + V_s}{L} t \tag{2.40}$$

$$i_L(\Delta t_4) = 0 \Rightarrow \Delta t_4 = t_4 - t_3 = \frac{I_{03} L}{V_o + V_s} \tag{2.41}$$

If desired, iterative techniques can be used to find Δt_i, i = 0, 1, 2, 3, 4, using the above results along with the equations,

$$\Delta t_o + \Delta t_1 + \Delta t_2 + \Delta t_3 + \Delta t_4 = T \tag{2.42}$$

$$\Delta t_3 + \Delta t_4 + \Delta t_o = t_{on} \tag{2.43}$$

2.2 Continuous Current Operation With Bypass

The circuit for the full bridge soft switch converter with an output bypass is shown in Fig. 1.5, while the detailed i_o waveform is shown in Fig. 2.7. The operation of the Q5 - Q6 bypass was described in the previous chapter.

$0 \le t \le t_o$: Q1, Q4 = on

$$\therefore I_{oo} = \frac{(V_s - V_o) t_o}{L} \tag{2.44}$$

$$\text{or } \Delta t_o = t_o = \frac{L I_{oo}}{(V_s - V_o)} \tag{2.45}$$

$t_o \le t \le t_1$:

If $i_{L(t_o)} < I_{x1}$, Q4 is not allowed to turn off when Q5 turns on. Therefore, Q1, Q4, Q5 = on. The equivalent circuit is shown in Fig. 2.8.

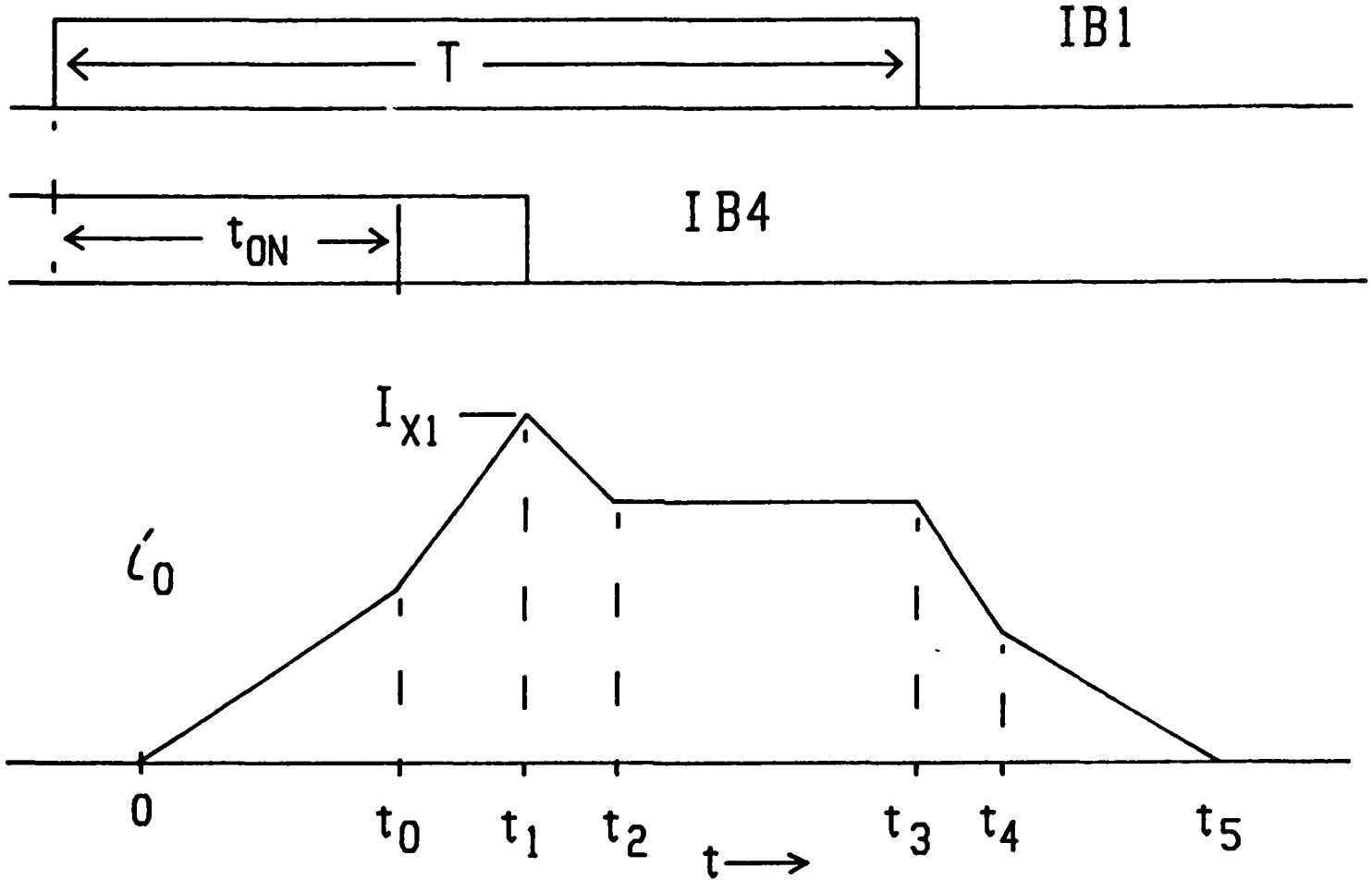


Fig. 2.7. i'_0 with bypass.

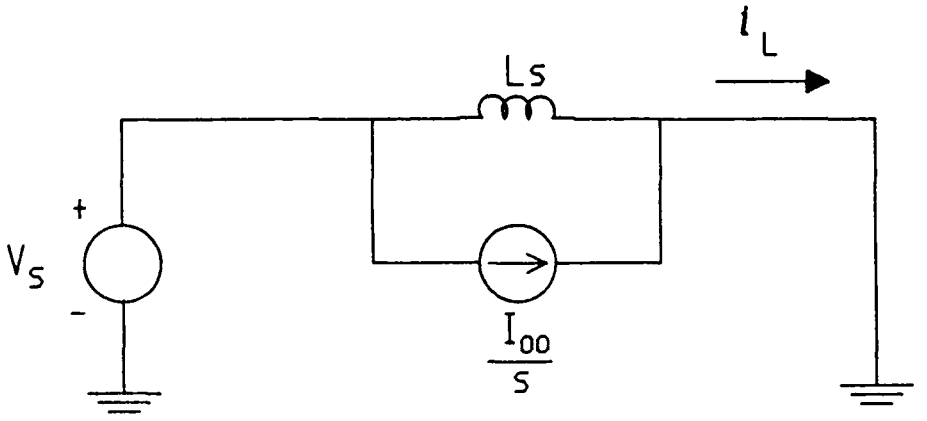


Fig. 2.8. Equlvalent circuit for $t_0 \leq t \leq t_1$.

From Fig. 2.8,

$$\frac{V_s}{s} = I_L Ls - I_{oo}L \tag{2.46}$$

$$I_L = \frac{V_s}{Ls^2} + \frac{I_{oo}}{s} \tag{2.47}$$

$$\therefore i_L = \frac{V_s}{L} t + I_{oo} \tag{2.48}$$

$$i_L(\Delta t_1) = I_{x1} = \frac{V_s}{L} \Delta t_1 + I_{oo} \tag{2.49}$$

$$\therefore \Delta t_1 = \frac{L(I_{x1} - I_{oo})}{V_s} \tag{2.50}$$

$t_1 \le t \le t_2$: Q4 = off, Q1, Q5 = on, C4 is charging. The equivalent circuit is shown in Fig. 2.9.

$$\frac{V_s}{s} = \frac{V_s}{s} + \frac{I_3}{Cs} - \frac{I_2}{Cs} \tag{2.51}$$

$$\therefore I_2 = I_3 \tag{2.52}$$

$$I_1\left(Ls + \frac{1}{Cs}\right) - I_{x1}L + I_2Ls = \frac{V_s}{s} \tag{2.53}$$

$$I_2\left(Ls + \frac{2}{Cs}\right) - I_{x1}L + I_1Ls - \frac{I_3}{Cs} = \frac{V_s}{s} \tag{2.54}$$

$$I_1\left(\frac{LCs^2 + 1}{Cs}\right) + I_2(Ls) = \frac{V_s}{s} + I_{x1}L \tag{2.55}$$

$$I_1(Ls) + I_2\left(\frac{LCs^2 + 1}{Cs}\right) = \frac{V_s}{s} + I_{x1}L \tag{2.56}$$

$$\therefore I_1 = I_2 \tag{2.57}$$

$$I_1\left(2Ls + \frac{1}{Cs}\right) = I_{x1}L + \frac{V_s}{s} \tag{2.58}$$

$$I_1 = \frac{I_{x1}s}{2\left(s^2 + \frac{1}{2LC}\right)} + \frac{V_2}{2L\left(s^2 + \frac{1}{2LC}\right)} \tag{2.59}$$

$$w_1 = \frac{1}{\sqrt{2LC}} \tag{2.60}$$

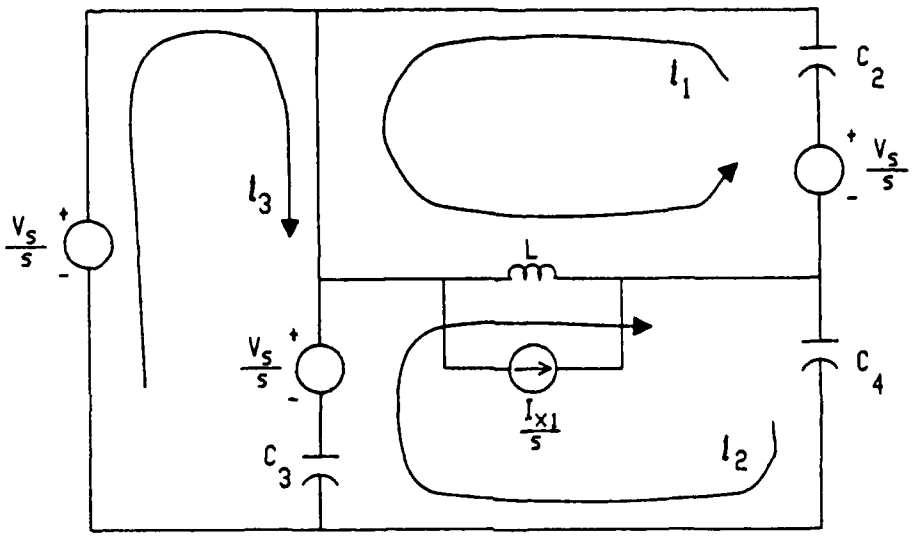


Fig. 2.9. Equlvalent circuit for $t_1 \leq t \leq t_2$.

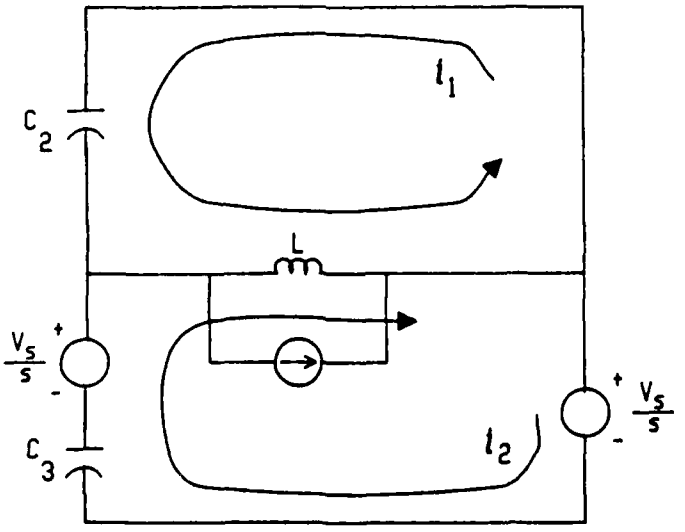


Fig. 2.10. Equlvalent circuit for $t_3 \leq t \leq t_4$.

$$i_1(t) = \frac{I_{x1}}{2} \cos w_1 t + \frac{V_s}{\sqrt{\frac{2L}{C}}} \sin w_1 t \tag{2.61}$$

$$\therefore i_1(t) = I_A \sin\left(w_1 t + \theta_1\right) \tag{2.62}$$

$$\text{where } I_A = \left[\frac{I_{x1}^2}{4} + \frac{CV_s^2}{2L}\right]^{1/2} \tag{2.63}$$

$$\theta_1 = \tan^{-1} \frac{I_{x1}\sqrt{\frac{2L}{C}}}{2V_s} \tag{2.64}$$

$$v_{C4} = V_s \Rightarrow v_L = 0 \tag{2.65}$$

$$\therefore v_L = L\left(\frac{di_1}{dt} + \frac{di_2}{dt}\right) = - \frac{2LI_A}{w_1} \cos\left(w_1 \Delta t_2 + \theta_1\right) = 0 \tag{2.66}$$

$$\text{or } w_1 \Delta t_2 + \theta_1 = \pi/2 \tag{2.67}$$

$$\therefore \Delta t_2 = \frac{\left(\frac{\pi}{2} - \theta_1\right)}{w_1} \tag{2.68}$$

$$I_{02} = i_{L(\Delta t_2)} = 2 I_A \sin\left(w_1 \Delta t_2 + \theta_1\right) \tag{2.69}$$

$t_2 \le t \le t_3$: Q1, Q5, D2 = on

L is shorted by Q1, Q5, and D2 so,

$$I_{03} = I_{02} \tag{2.70}$$

$t_3 \le t \le t_4$: Q1 = off, C1 charges, C3 discharges, Q5, D2 = on.

The equivalent circuit is shown in Fig. 2.10.

For the i_1 loop,

$$I_1\left(Ls + \frac{1}{Cs}\right) - L I_{03} + I_2 Ls = 0 \tag{2.71}$$

For the i_2 loop,

$$I_2\left(Ls + \frac{1}{Cs}\right) - L I_{03} + I_1 Ls = 0 \tag{2.72}$$

$$\therefore I_1 = I_2 \tag{2.73}$$

$$\therefore i_1(t) = \frac{I_{02}}{2} \cos w_1 t \tag{2.74}$$

D3 turns on @ $t = \Delta t_4$ when,

$$v_L = V_s = L\left(\frac{di_1}{dt} + \frac{di_2}{dt}\right) = - L I_{03} w_1 \sin w_1 t \tag{2.75}$$

$$\therefore \Delta t_4 = \frac{1}{w_1} \sin^{-1}\left(\frac{V_s}{w_1 L I_{03}}\right) \tag{2.76}$$

$$\text{and } I_{04} = i_1(\Delta t_4) + i_2(\Delta t_4) = I_{03} \cos\left(w_1 \Delta t_4\right) \tag{2.77}$$

$t_4 \le t \le t_5$: D2, D3 = on, L dumps its energy into V_s.

From Fig. 2.11,

$$i_L(t) = I_{04} - \frac{V_s}{L} t \tag{2.78}$$

$$i_4(t_5) = 0 \Rightarrow \Delta t_5 = \frac{I_{04} L}{V_s} \tag{2.79}$$

As for the case with no bypass, iterative techniques can be used to find Δt_i, $i = 0, 1, 2, 3, 4, 5$ using the above results along with the equations,

$$\Delta t_o + \Delta t_1 + \Delta t_2 + \Delta t_3 + \Delta t_4 + \Delta t_5 = T \tag{2.80}$$

$$\Delta t_4 + \Delta t_5 + \Delta t_o = t_{ON} \tag{2.81}$$

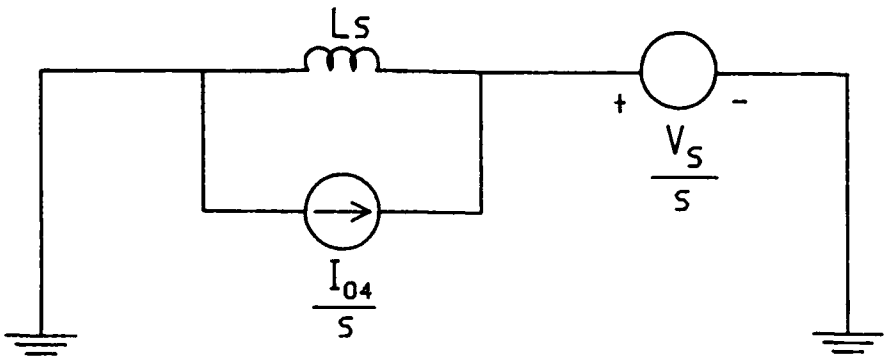


Fig. 2.11 Equlvalent circuit for $t_4 \leq t \leq t_5$.

III. CURRENT MODE CONTROL FOR THE FULL BRIDGE CONVERTER

3.1 Advantages of the CMC Full Bridge

As the problems with the bypass converter became more apparent, several other full bridge topologies were reviewed for the sake of comparison. Because of the relatively low switching losses of currently available FETs and IGTs, it was decided to concentrate on converters using forced commutation. One class of these circuits uses reactive components (L, LC or C) in series with the transformer primary, to overcome the flux imbalance problem and aid in short circuit protection. The size, cost and parasitic losses of these components was considered undesirable however, so it was decided to explore the use of current mode control (CMC) for the full bridge.

Therefore, the basic reason for concentrating on CMC can be summarized in the following manner. Converters with series L, LC, or C depend on this reactance to compensate for transformer flux imbalance and aid in short circuit protection. This usually seems to work, but at the expense of a large (and sometimes lossy) component(s). CMC eliminates flux imbalance and provides short circuit protection by sensing the instantaneous primary current. Thus a CMC converter should be smaller, but the controller is more complex (although not nearly as complex as the bypass controller). The primary goal was to determine if the CMC would be feasible for a full bridge converter at higher power levels.

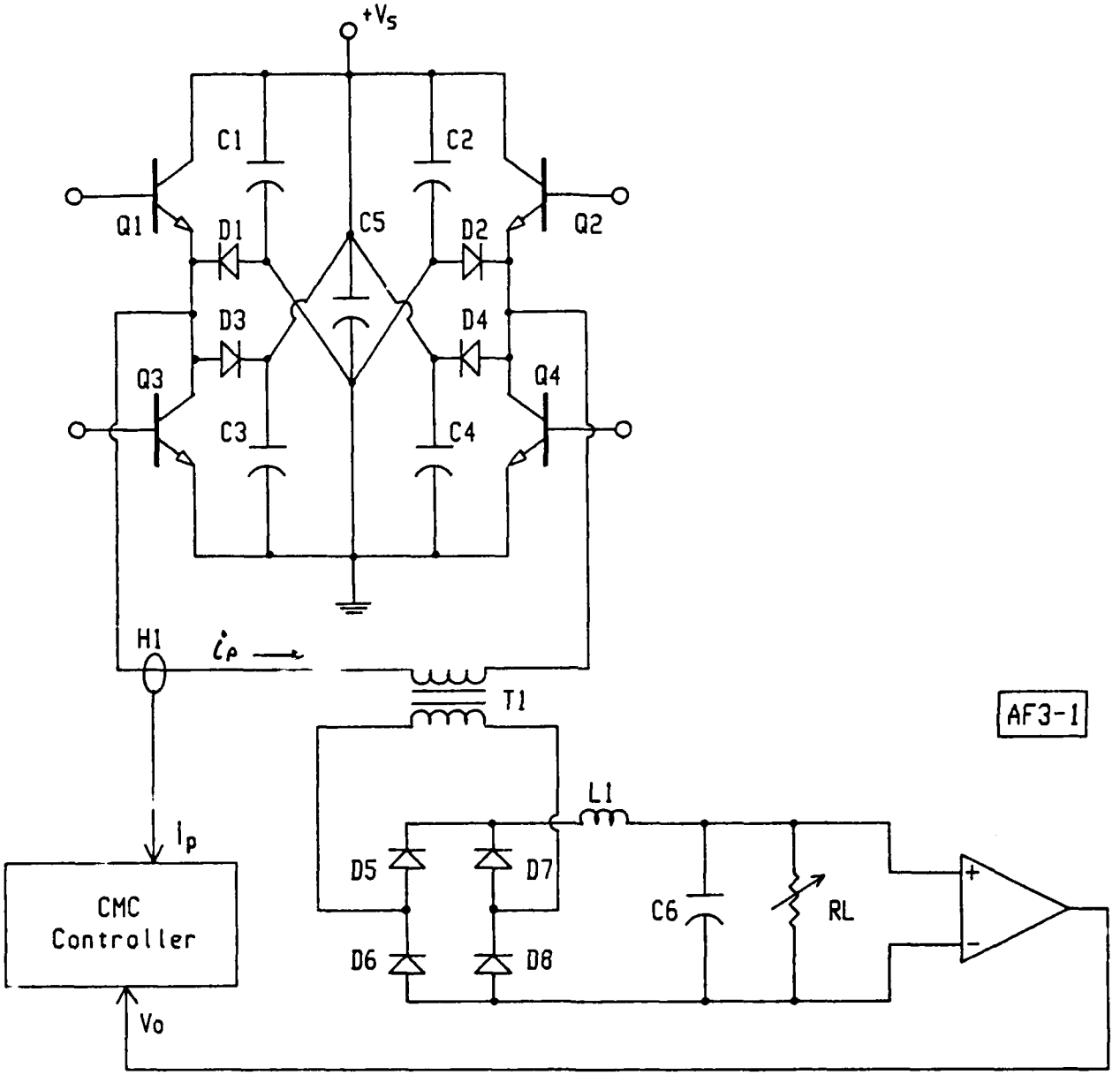
3.2 Current Sensing Methods

Although CMC is considered to be a well known control technique, very little technical literature was found for the full bridge versions. One possible reason for this soon became apparent however, when certain difficulties were

encountered in sensing the current waveform for the CMC controller. The basic problem is to find a sensing method that measures the dc imbalance without an undo amount of EMI. However, three acceptable current sensing methods were developed after extensive effort, and preliminary results are quite encouraging. Because of this success, and the unresolved problems with the bypass converter, it appears that the full bridge CMC with one of these new sensors may provide a much better converter.

The basic schematic of a CMC full bridge converter is shown in Fig. 3.1. Instead of dissipative snubbers, this circuit uses a voltage clamp for each IGT. Minimum lead lengths for the clamp components are quite important for this circuit, so the schematic is drawn to emphasize component location. As with any CMC controller, it is necessary to monitor the instantaneous value of i_p. This particular circuit used a Hall effect device, H1, for this function. The Hall device is necessary because the controller must be able to sense any DC imbalance in the i_p waveform. This precludes the use of a current transformer (CT) in series with the primary of T1.

Another current sensor capable of monitoring the DC imbalance is shown in Fig. 3.2. This circuit uses a CT with two primaries, each in series with a separate leg of the bridge. The CT acts like a pulse transformer on each half cycle. For example, the current amplitude is monitored while Q2 and Q3 are on, and the CT core flux is reset to zero by a relatively high amplitude, short duration fly-back pulse across D9 when i_p reaches zero. A similar process occurs during the next half cycle when Q1 and Q4 conduct. This circuit has certain advantages in that it has relatively low temperature drift and requires less initial



H1=Hall effect device

Fig. 3.1. Full bridge CMC converter with Hall effect sensor.

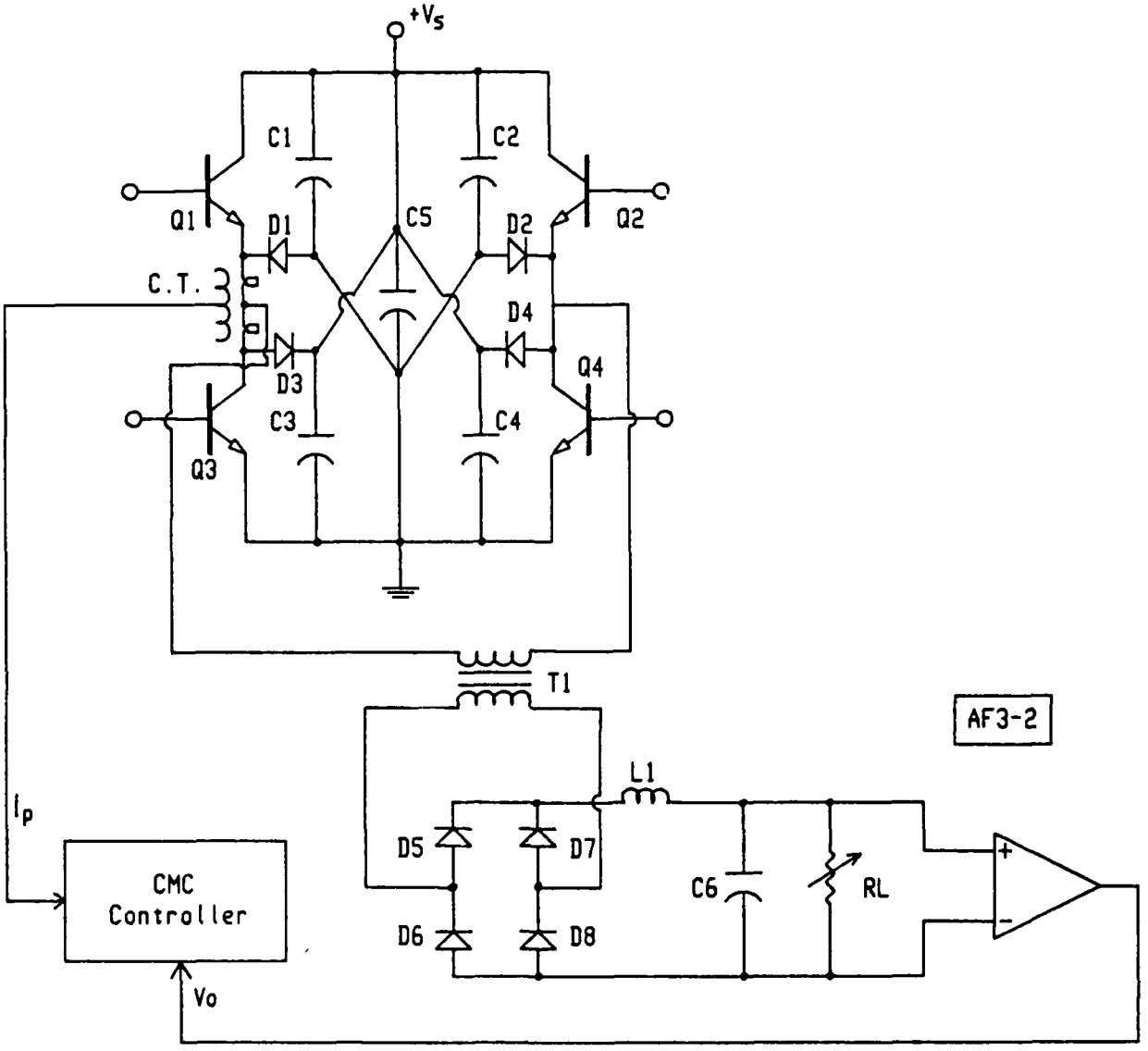


Fig. 3.2. Full bridge CMC converter with dual primary C.T.

calibration than a Hall sensor. Preliminary experimental results indicate that the transient response of the converter is more oscillatory than with a Hall sensor however, and this characteristic is still under investigation.

The third current sensing arrangement that was tested is shown in Fig. 3.3. This system uses two CT's, one in each leg of one side of the bridge. Since there may be variations between the two CT's, experimental results indicate that the two CT signals must be balanced with a potentiometer. This is a disadvantage that is not present in the single CT circuit, but it is not a serious one since the balance adjustment is quite simple. The main advantage of this circuit over the single CT with dual primaries is that its transient response does not seem to exhibit any oscillatory behavior. The exact reason for this is not yet clear and is the subject of a continuing study.

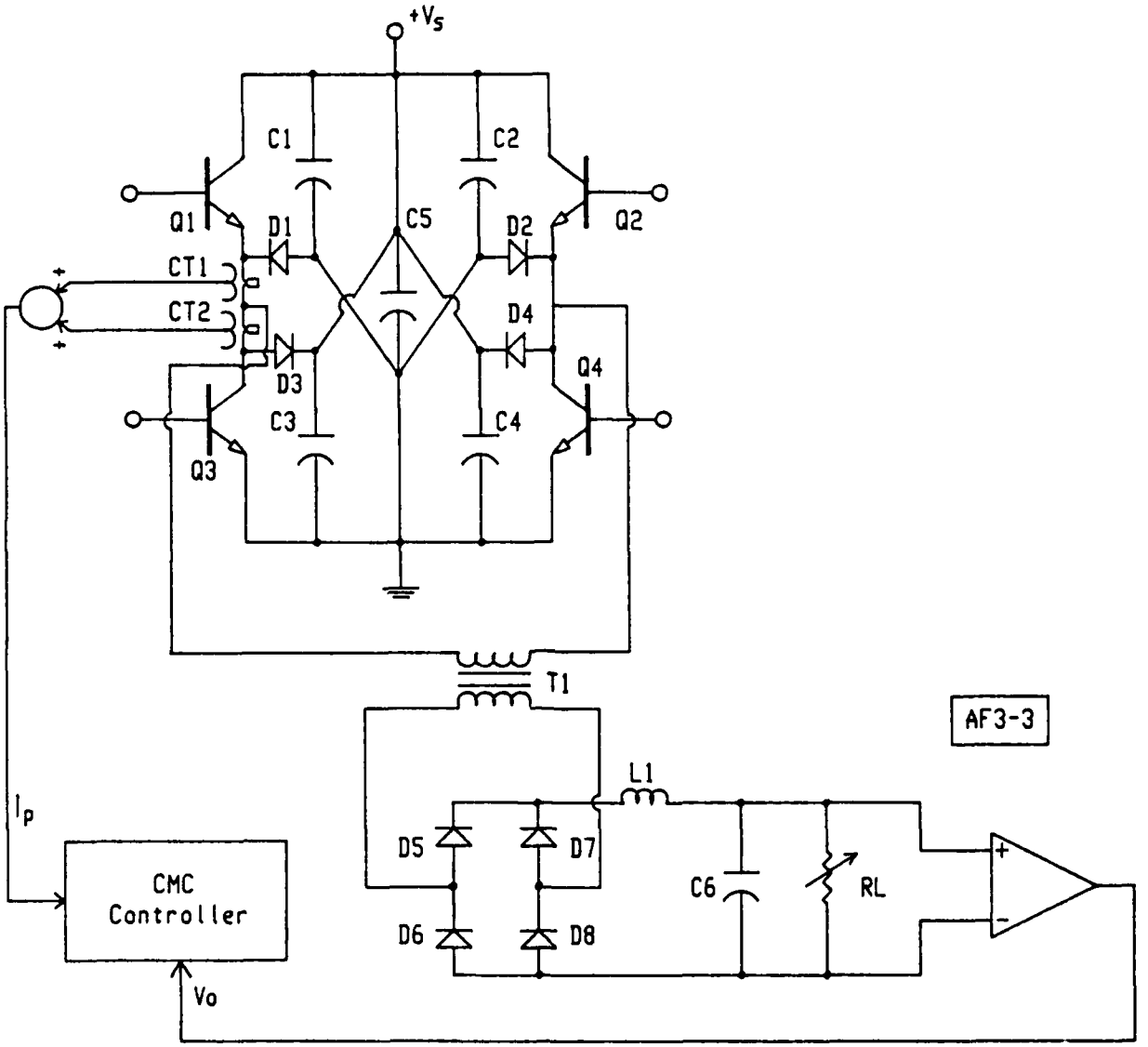


Fig. 3.3. Full bridge CMC converter with two C.T.'s

IV. EXPERIMENTAL RESULTS

4.1 Soft-Switch Bypass Converter

The original intent of this project was to determine the feasibility of a new soft switch converter which bypasses the load during part of the switching cycle. A 180 watt 20 KHz version of the circuit was built, tested, and compared with a more conventional current mode control (CMC) converter. A block diagram of the bypass system is shown in Fig. 4.1, while individual schematics are shown in Figs. 4.2 through 4.4.

Although the bypass circuit proved functional, certain problems were uncovered which raise doubts about its ultimate feasibility. One problem is that the controller is fairly complex, indicating that most applications will require a highly skilled designer. Another problem is a randomly occurring mode where the conduction intervals for the two sides of the bridge become highly unbalanced. Finally, the most important drawback may be the fact that the actual measured efficiency did not appear to be any better than conventional PWM.

The conclusion was that the bypass circuit presents some complex problems but no clear advantage over CMC. Because of this, it was decided to concentrate on developing a full bridge version of the CMC instead of the bypass circuit.[1] Although the bypass development was truncated at an early stage, a brief description of the 180 watt version is included to illustrate some of the problems and explain why some of the anticipated advantages were not realized.

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1. Although there is considerable technical literature on CMC, very little has been published on full bridge versions [9.]. This may be due in part to problems with the current sensor which will be discussed later.

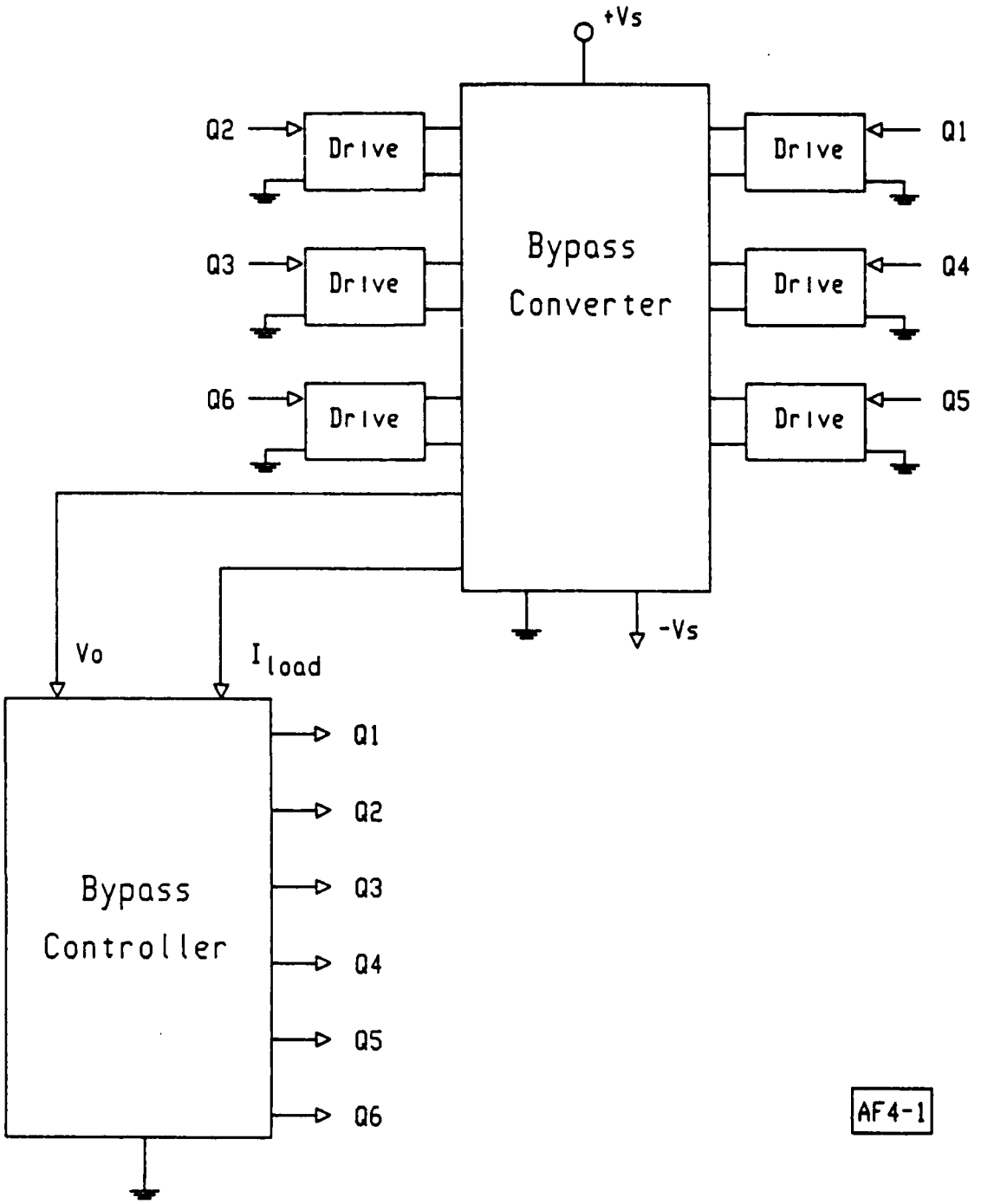

Fig. 4.1. Block diagram of bypass converter with controller.

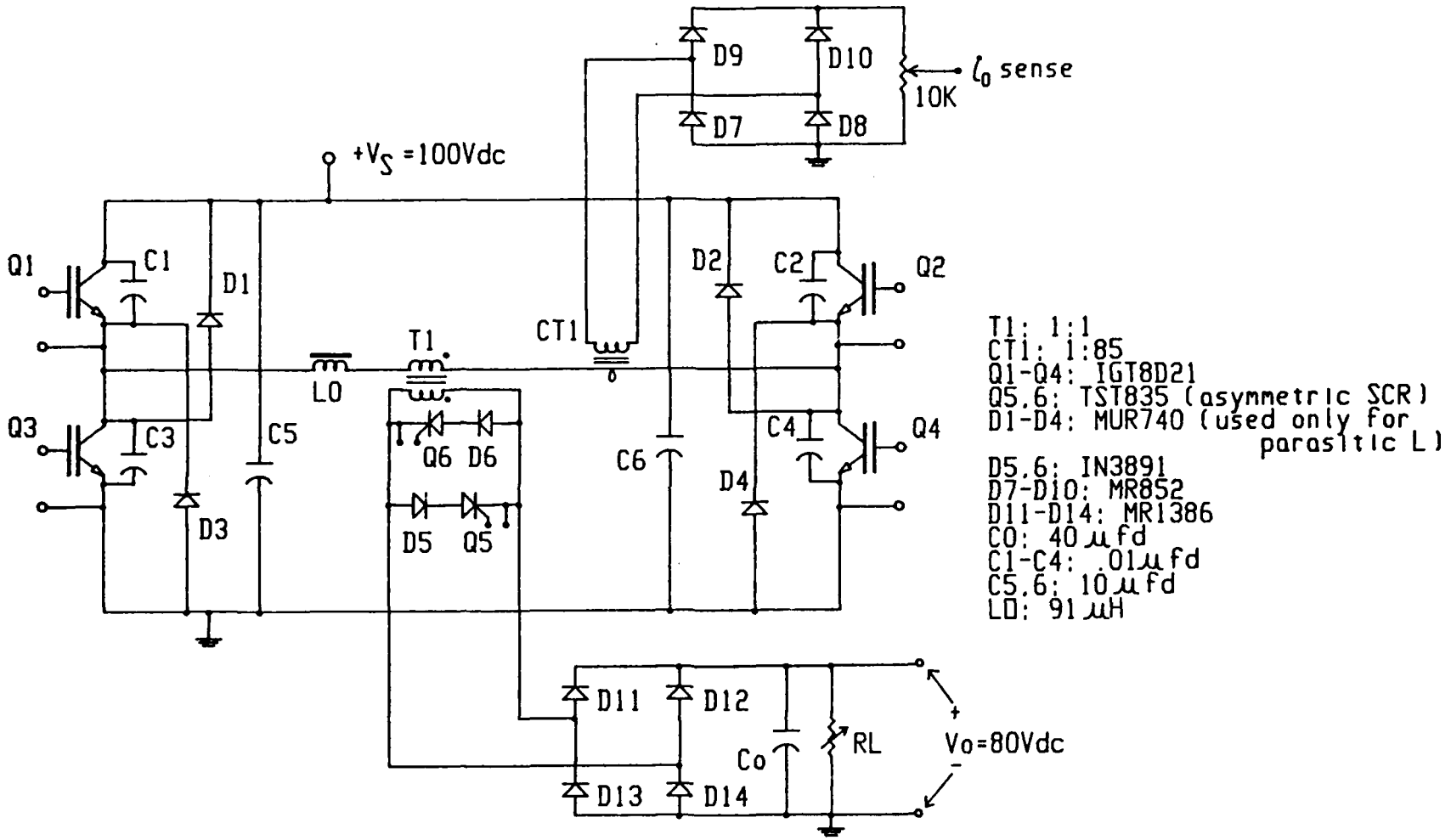

Fig. 4.2. Bypass converter.

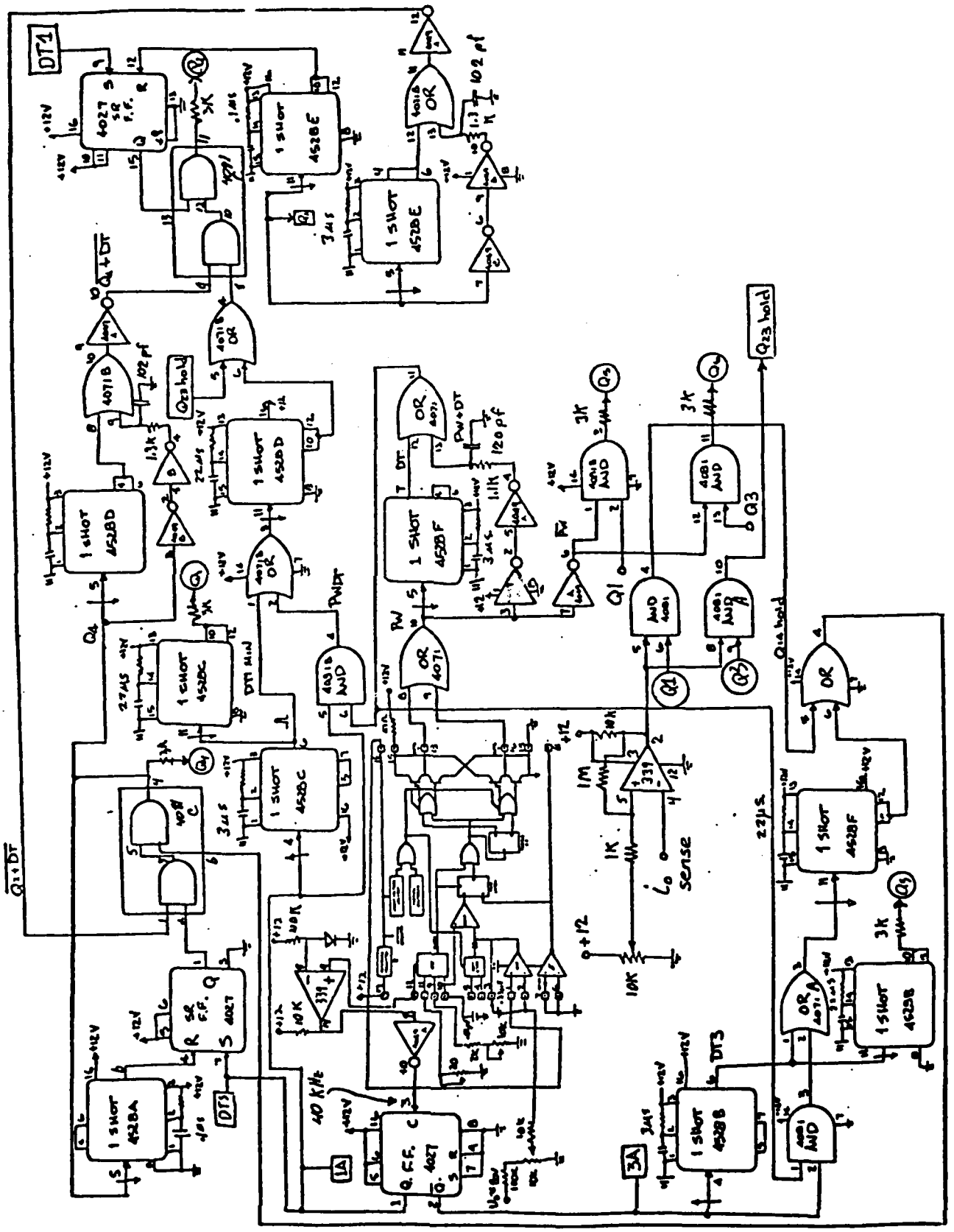

Fig. 4.3 Control circuit for bypass converter

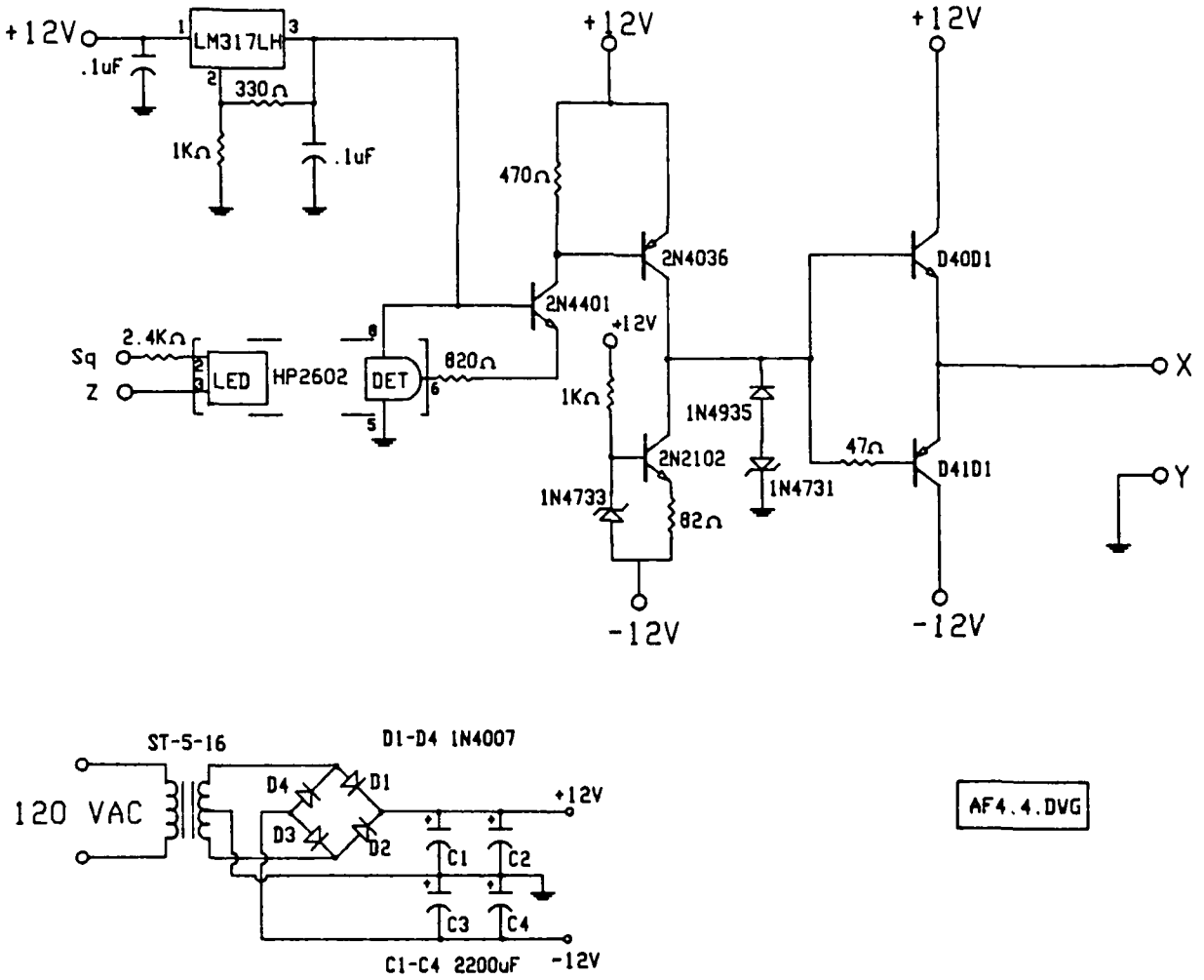

FIG.4.4 IGT GATE DRIVE

At 20 kHz, the 180 watt circuit in Fig. 4.2 had an efficiency of around 90%. This is about the same as that of a comparable CMC converter. Because of soft switching, the switching losses in Q1-4 are probably less than those of a CMC circuit, but other losses are higher. These losses include higher conduction loss due to the higher peak currents and much higher losses in L_o , which sees a high AC current. Q5-6 and D5-6 also present additional conduction losses during the bypass portion of the operating cycle. One reason that the lower switching losses do not have a more pronounced effect is that they are already fairly low at 20 kHz, even with forced commutation. This is due to the re-latively low fall times of the newer IGTs.

Another problem with the circuit in Fig. 4.2 was to find satisfactory bypass switches, Q5 and Q6. Towards the end of a half cycle after the capacitors are charged, L_o must dump its remaining energy into V_s via D2, D3, D5, Q5 or D1, D4, D6, Q6. Since the length of this remaining portion of the cycle is variable, it is more convenient to use SCRs for Q5 and Q6 instead of a self commutation device such as an IGT. One device that can perform this function at 20 kHz is an asymmetric SCR, such as the TST835 which was used. Unfortunately, this device has very limited reverse voltage blocking capability. Therefore, it was necessary to add the blocking diodes D5 and D6, which further increases the conduction losses. The only type of switch that has an adequate reverse voltage rating is the conventional SCR, but this device is too slow for 20 kHz operation.

Another problem that should be noted is the relative complexity of the bypass controller in Fig. 4.3. Although the control strategy is conceptually simple, its implementation is a formidable challenge. This presents numerous

opportunities for logic errors and tends to decrease the overall reliability of the circuit.

4.2 Full Bridge CMC Converter

The circuit for a 1kW, 20 kHz converter is shown in Fig. 4.5. The controller for the version with the Hall effect i_p sensor is shown in Fig. 4.6. The details for the CT i_p sensor with dual primaries is shown in Fig. 4.7, and the schematic for the i_p sensor with two CT's is shown in Fig. 4.8. The IGT gate drive circuit is the same as that shown in Fig. 4.4.

Measured full load efficiency at 1 kW, V_s =140 Vdc, V_o =200 Vdc was 91.3%. The open loop gain and phase was measured by interrupting the voltage feedback loop at point A in Fig. 4.6. The results are plotted in Figs. 4.9 and 4.10. Figs. 4.11 and 4.12 show the same information for a load of 200 watts. These plots indicate the phase margin at 1 kW is about 30°, and at 200 W. it is about 22° . No oscillations were observed over the load range of 0 to 1 kW.

A few waveforms if interest are shown in Figs. 4.13 through 4.16. Figs. 4.13 and 4.14 show the i_p waveform. These waveforms indicate that no transformer saturation occurs since there is no evidence of the current "curling up" to a peak just before turn-off. Figs. 4.15 and 4.16 show the collector-emitter voltage of one of the IGT's along with its collector and voltage clamp current (collector current could not be measured separately because of the short lead length between the IGT and the clamp). The v_{CE} waveform shows only a slight overshoot, indicating the effective-ness of the voltage clamp.

While all three i_p sensing methods appear to be satisfactory, there are some

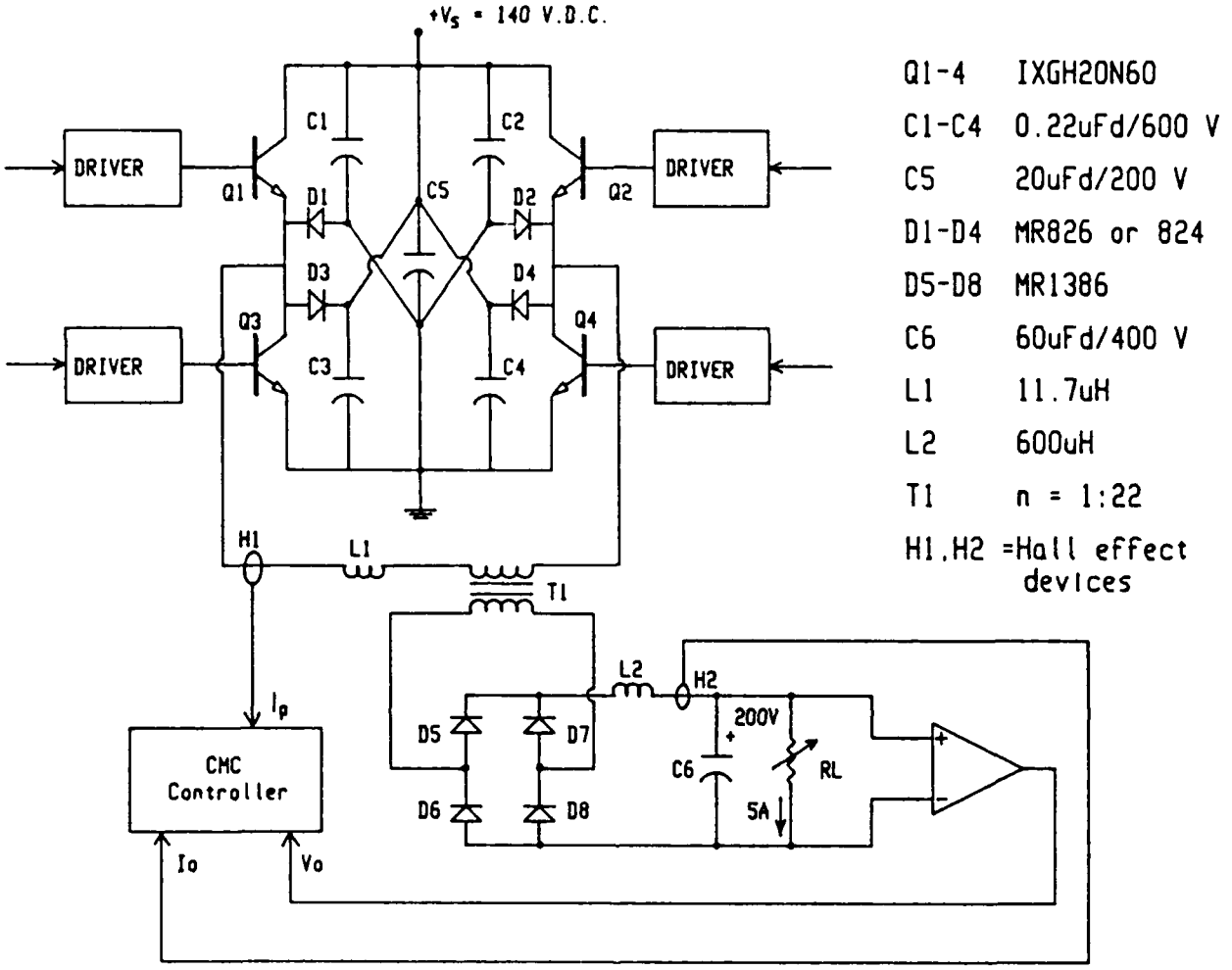

FIG 4.5 Full bridge CMC converter (Hall effect version)

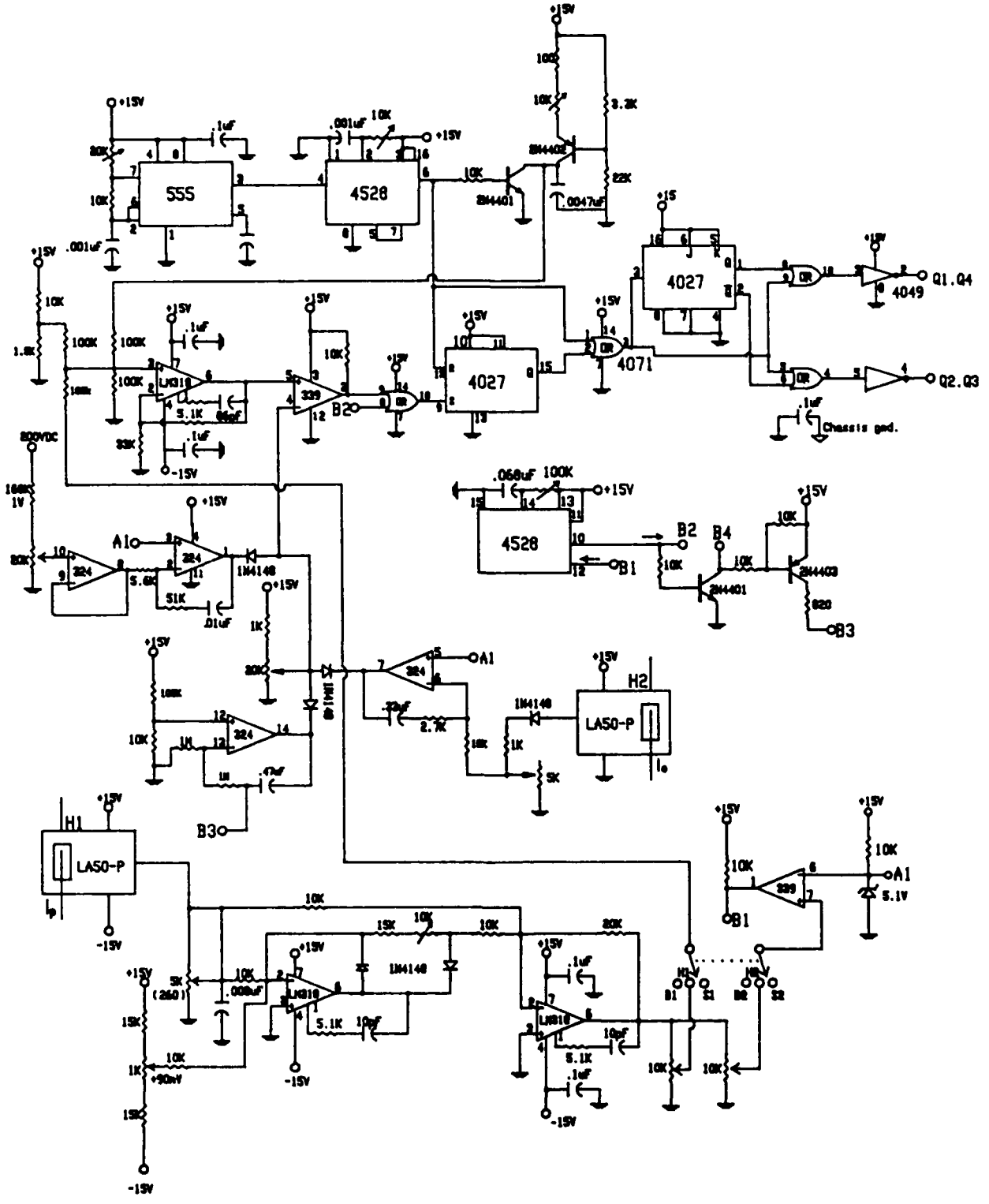

Fig. 4.6 CMC controller with Hall effect sensor for Ip

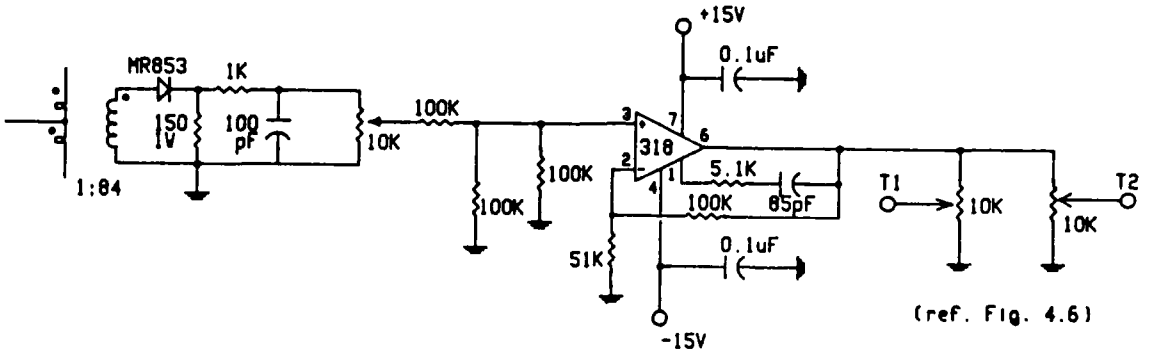

Fig. 4.7 Ip sensor using C.T. with dual primaries

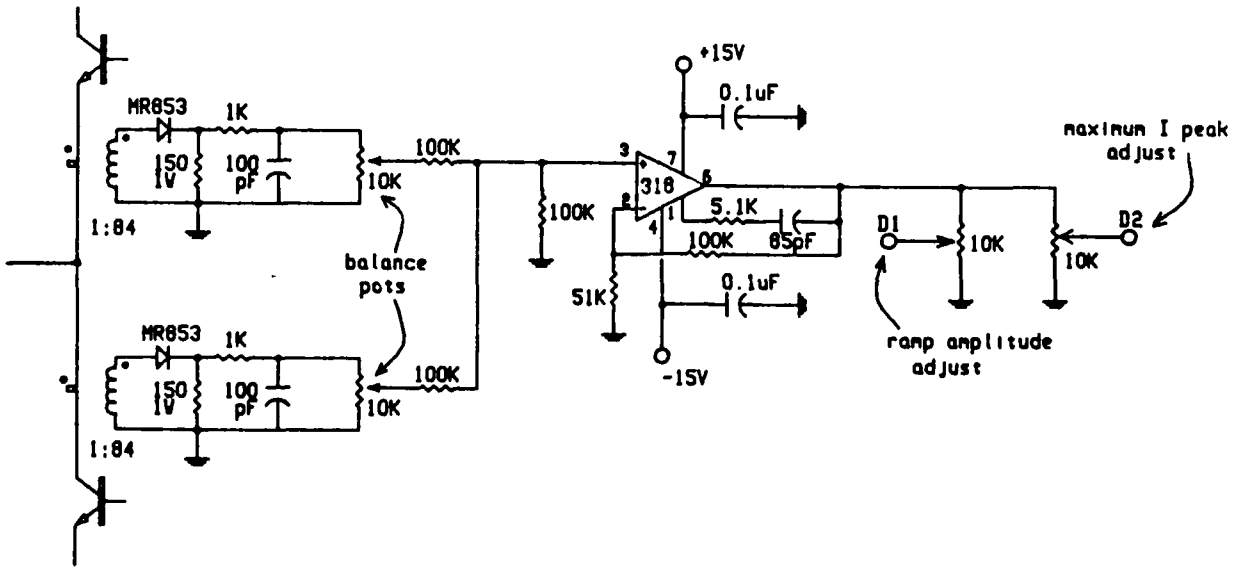

Fig. 4.8 Ip sensor using two C.T.s

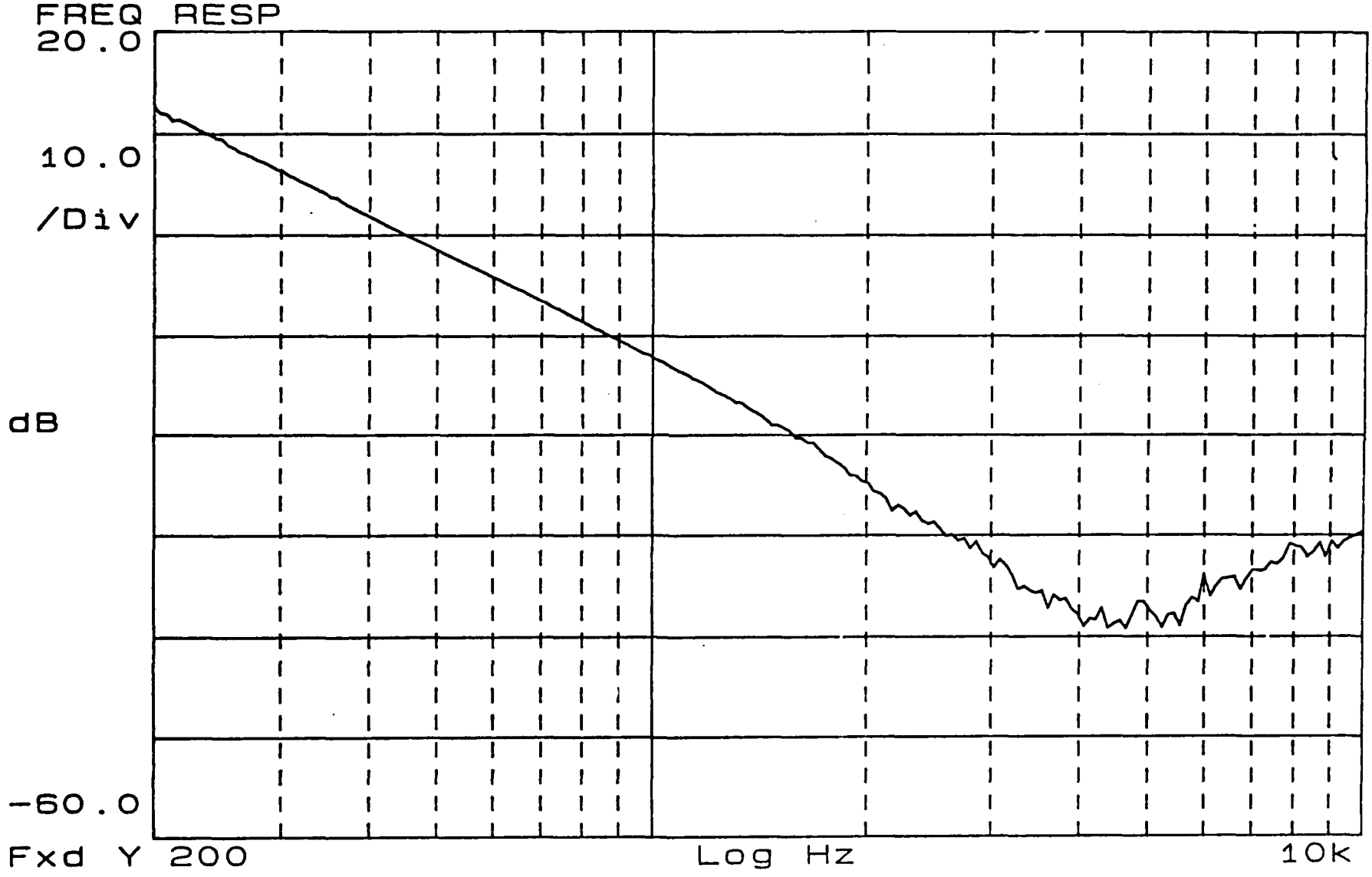

Fig. 4.9. Open loop gain for the full bridge CMC converter with the dual C.T. current sensor. V_S = 140 Vdc, V_O = 200 Vdc, I_O = 5.0 Adc.

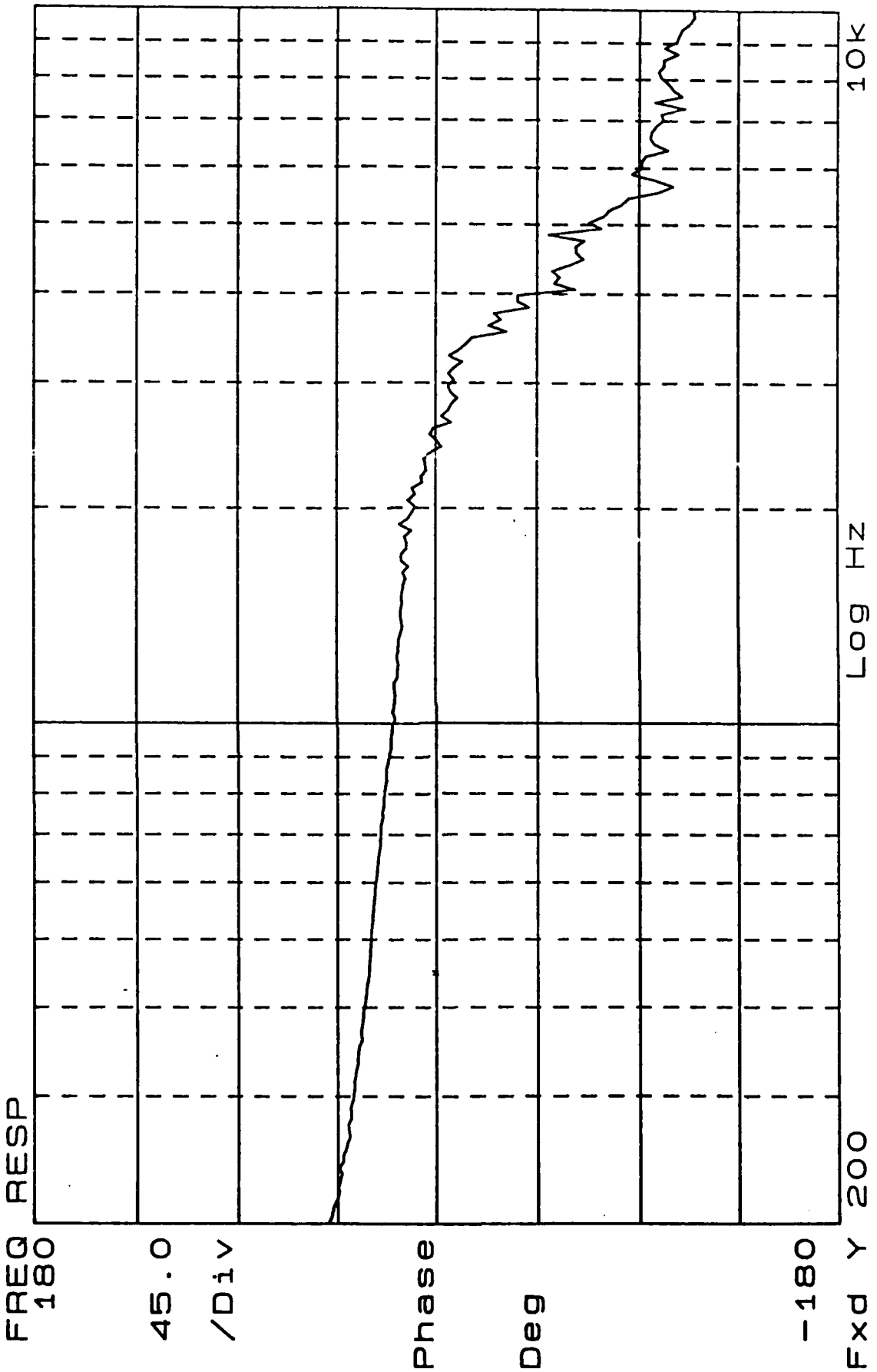

Fig. 4.10. Open loop phase shift for the same conditions as Fig. 4.9.

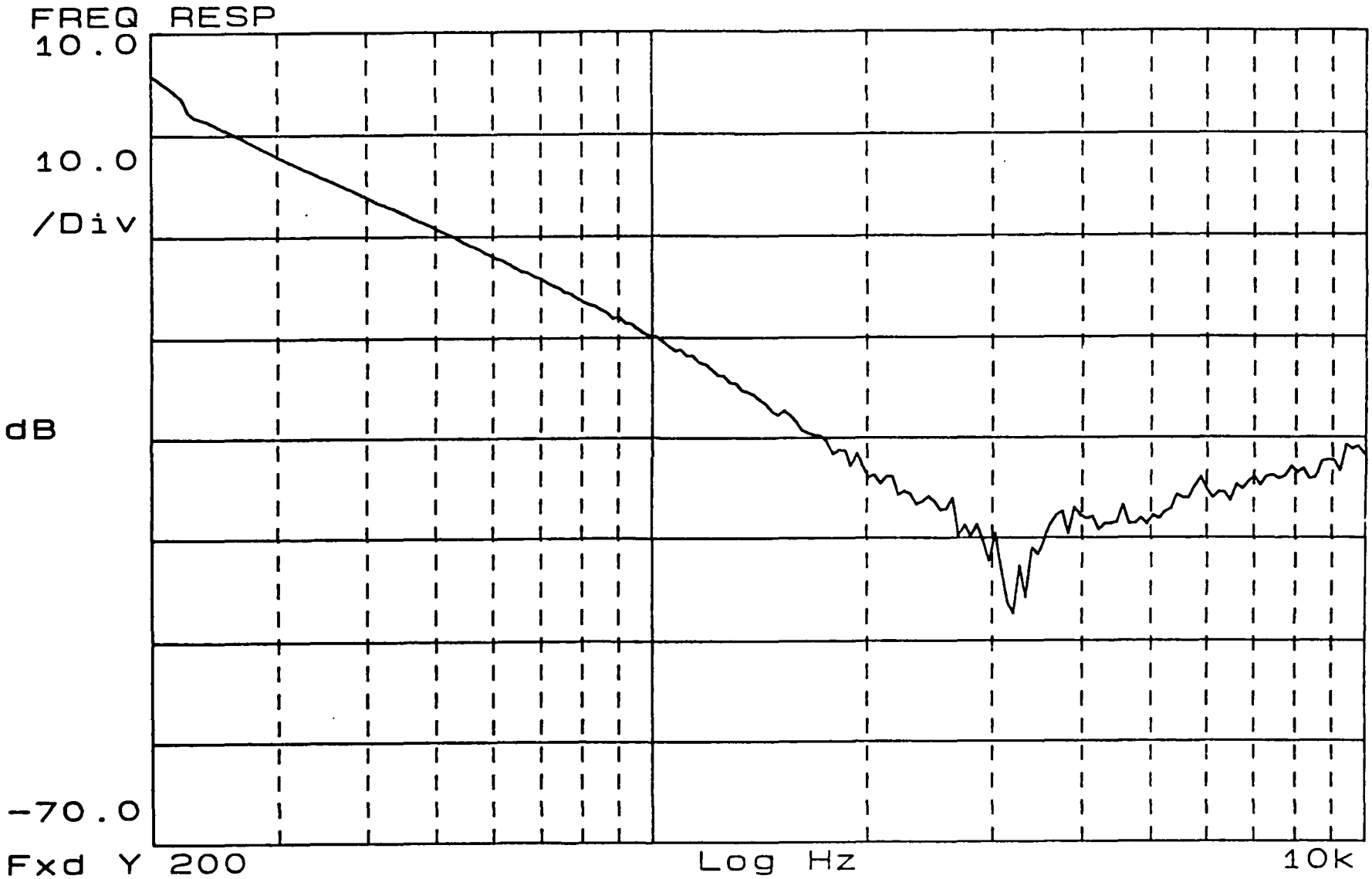

Fig. 4.11. Open loop gain for the full bridge CMC converter with the dual C.T. current sensor. V_s = 140 Vdc, V_o = 200 Vdc, I_o = 1.0 Adc.

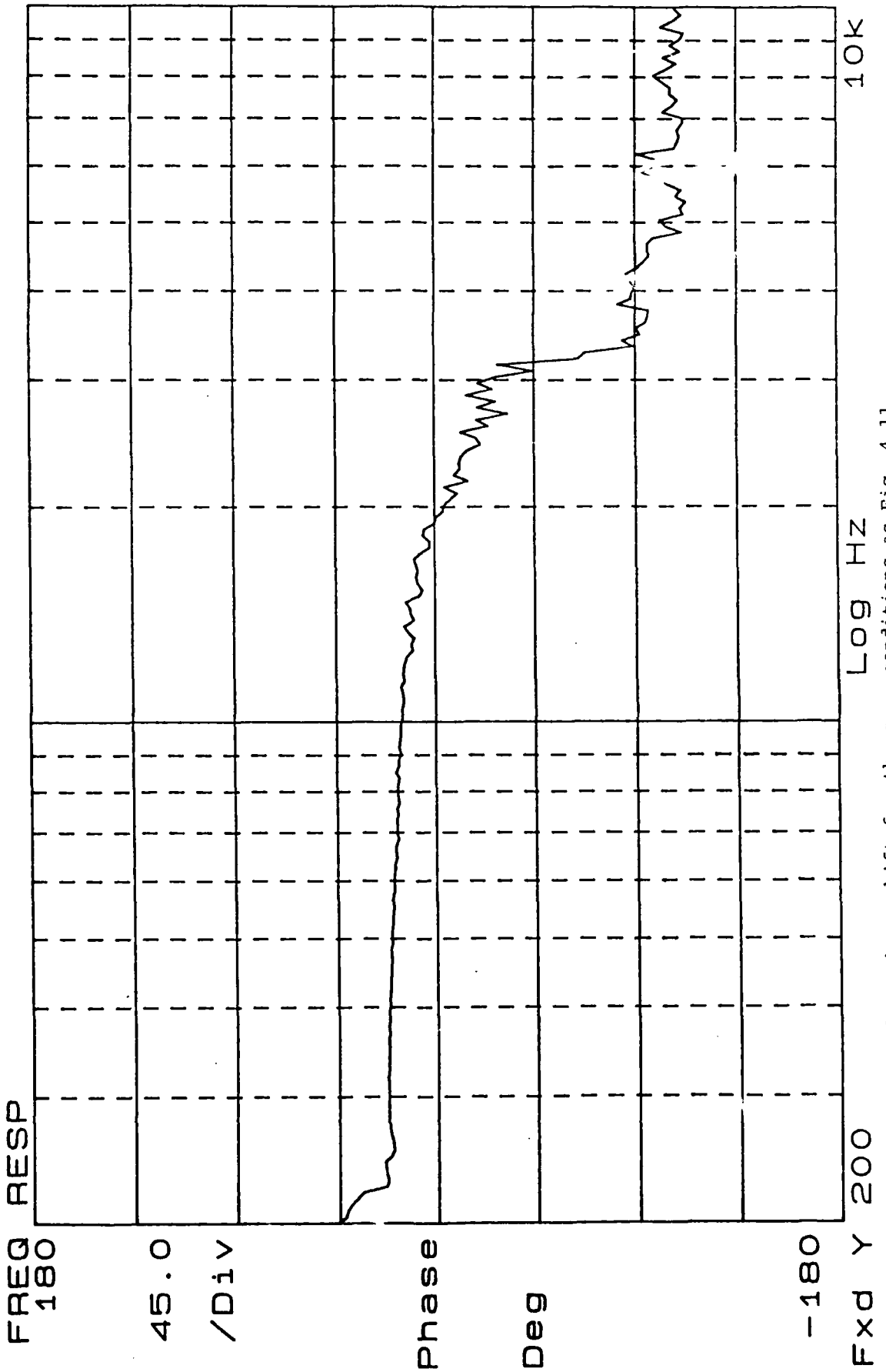

Fig. 4.12. Open loop phase shift for the same conditions as Fig. 4.11.

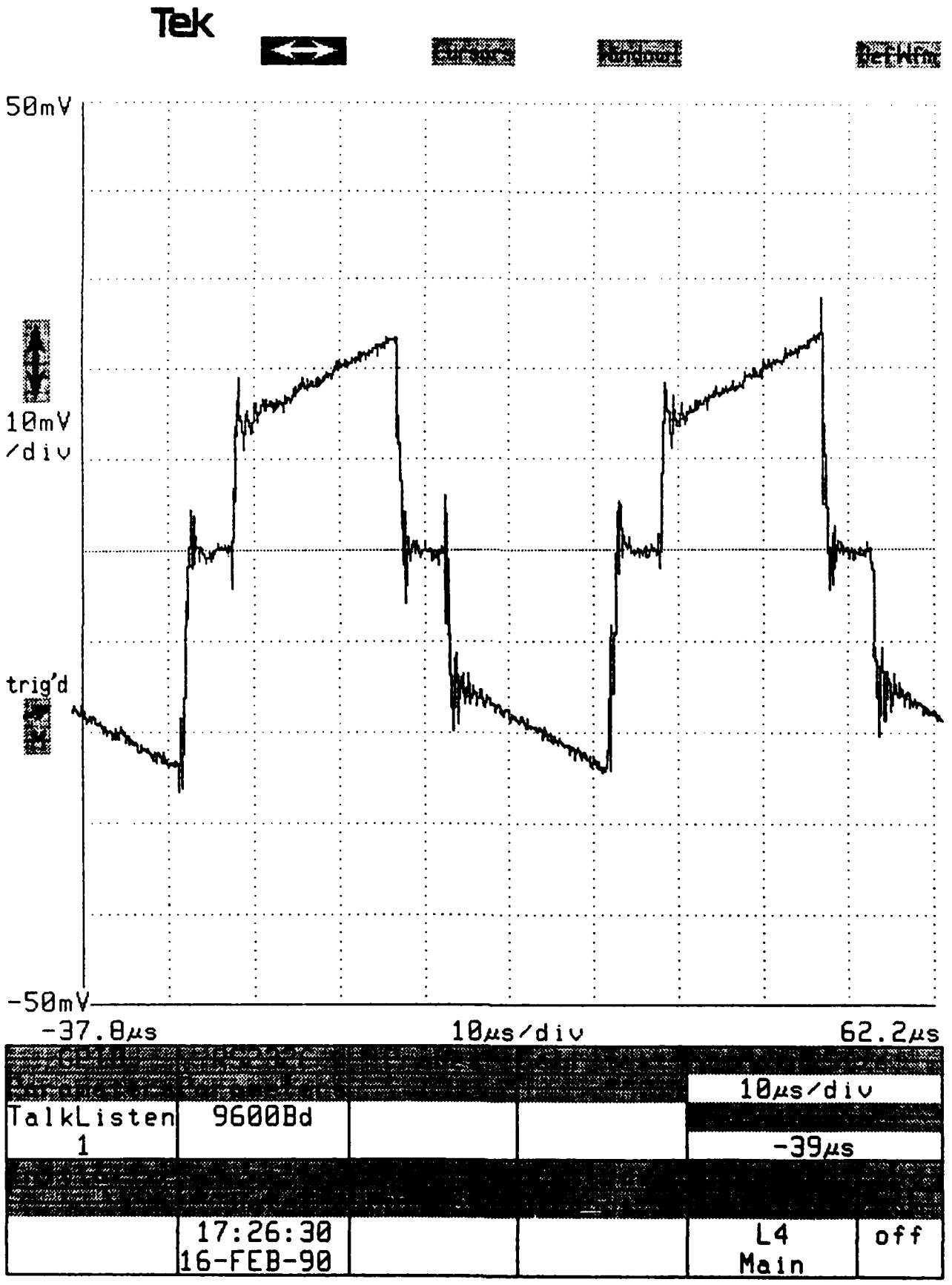

Fig. 4.13. i_p for full bridge CMC with dual primary C.T.

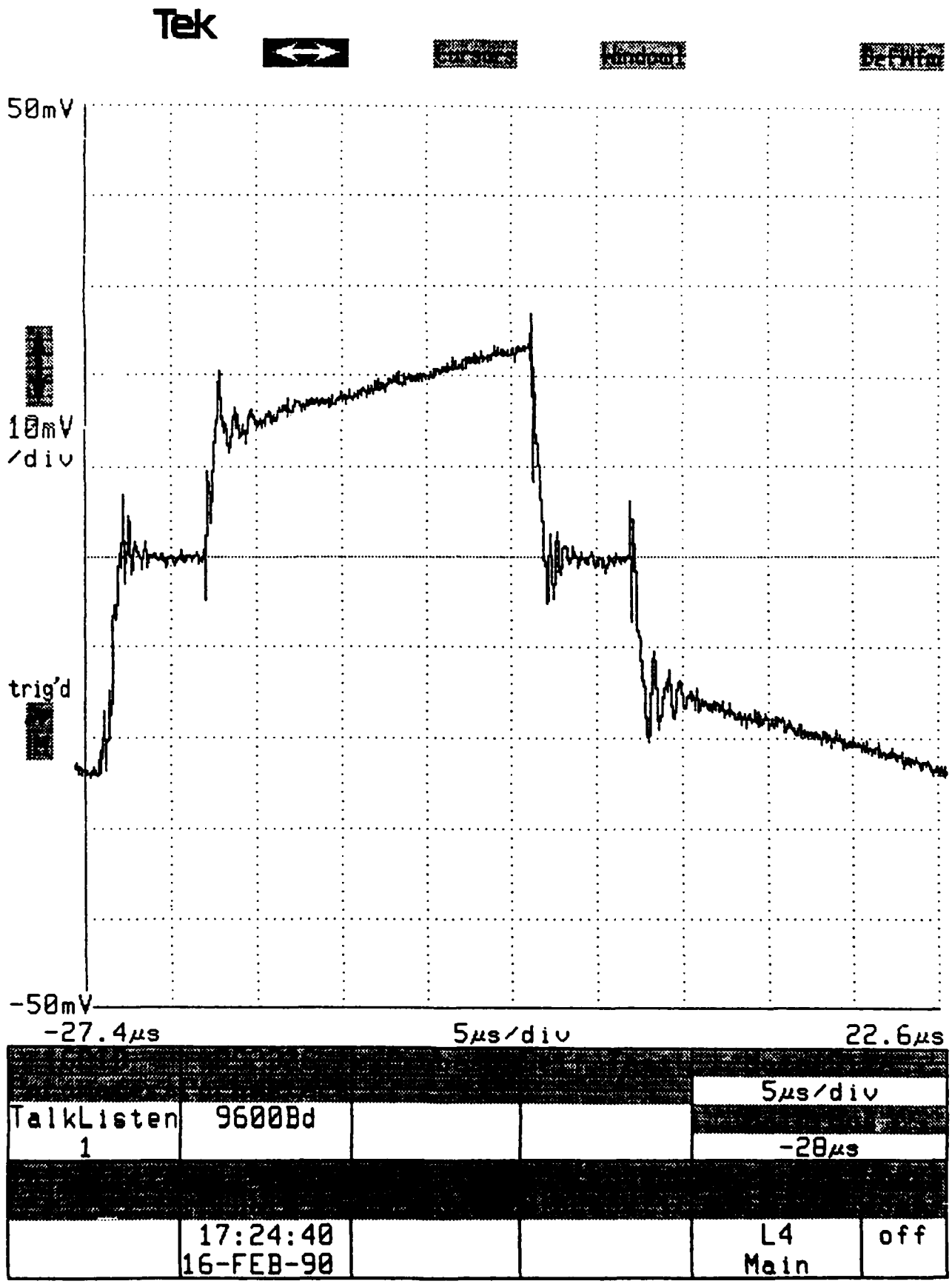

Fig. 4.14. i_p waveform similar to Fig. 4.13 with expanded time scale.

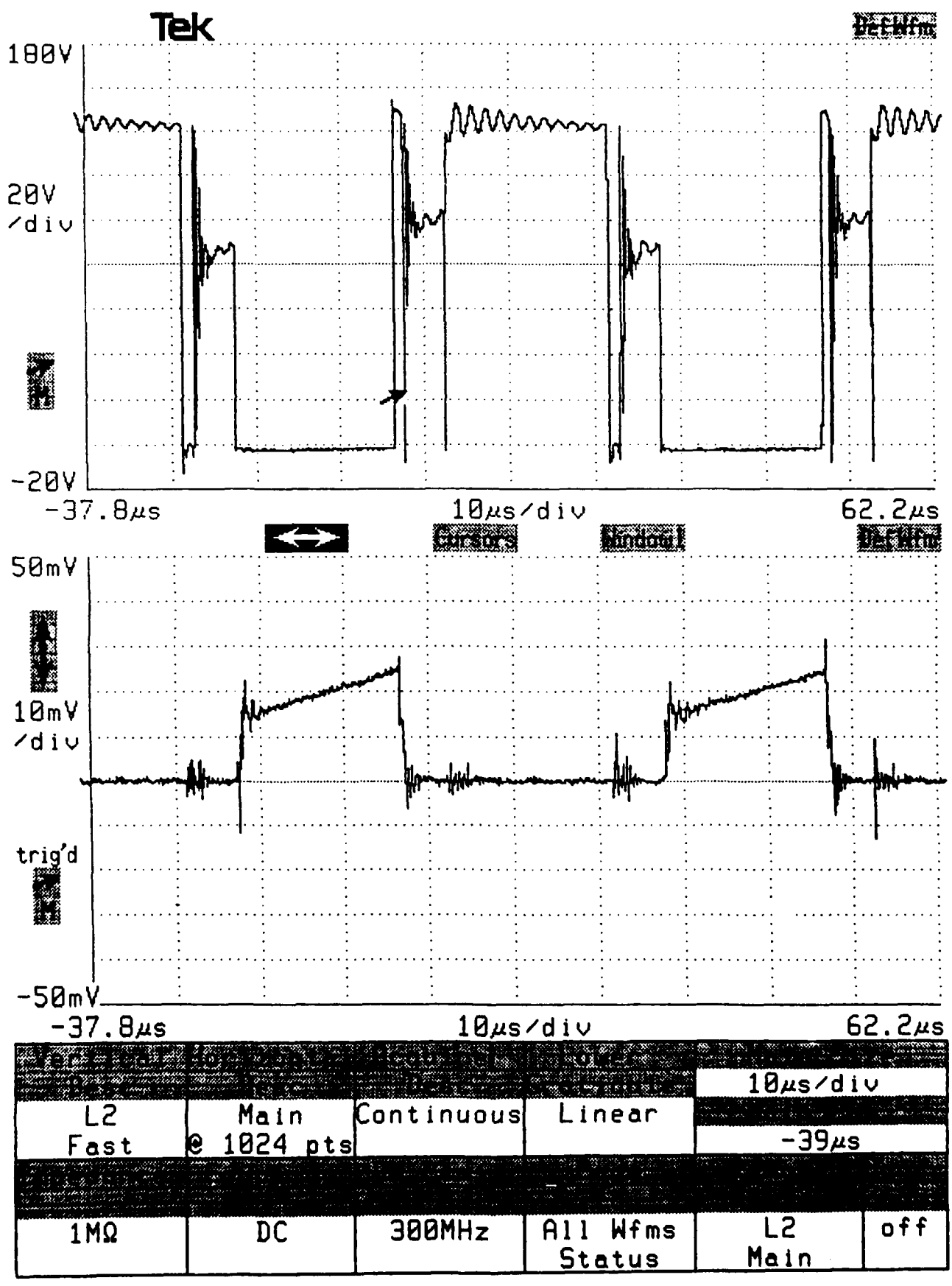

Fig. 4.15. Top: Collector-emitter voltage. Bottom: Current in collector & voltage clamp.

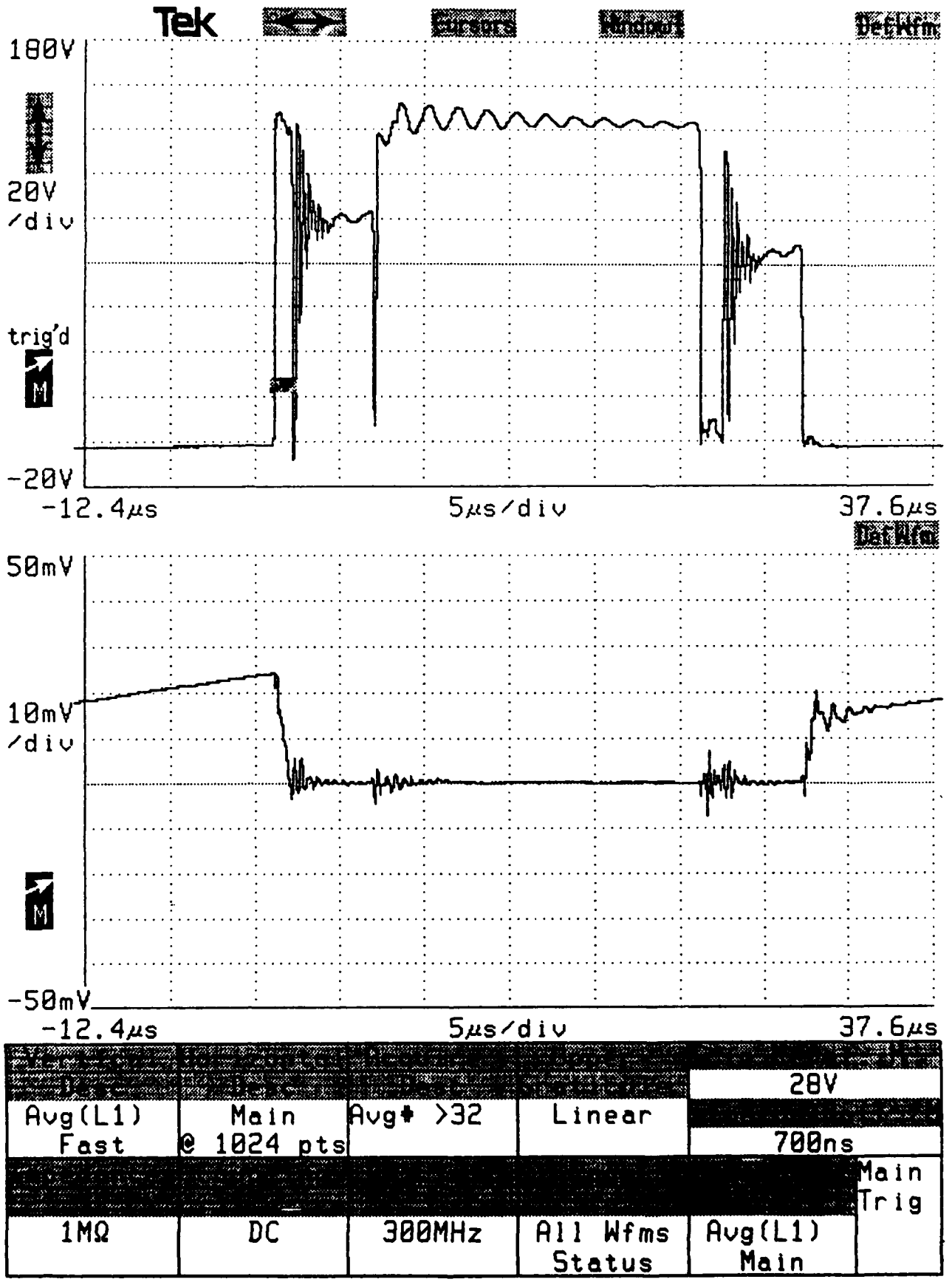

Fig. 4.16. Same waveforms as Fig. 4.15 with expanded time scale.

remaining questions that need further investigation. On first examination it would appear that the dual primary CT would provide the optimum method. It is the simplest, and it requires no calibration to prevent transformer saturation. It was observed, however, that the sensor tends to produce a slightly oscillatory response to a step change, such as at initial turn-on. This oscillatory response was not observed when two CT's were used, but this sensor requires balancing because of slight differences in the two CT's and their associated circuitry. The Hall effect sensor did not display any oscillatory response, but it too requires a balancing calibration because of initial offset and slight imbalances in the absolute value circuit used to rectify the waveform. According to its specifications, the offset voltage of the Hall effect device may drift with temperature. The sensor was temperature cycled from 25℃ to 100°C (only rated to 70°), but whatever drift occurred did not create any evidence of transformer saturation.

V. SUMMARY

The soft-switch converter with the output bypass proved to be functional, but the random imbalance problem and lack of realized advantages cast doubts about its feasibility. The full bridge CMC converter appears to be a much more viable cir cuit, and further development may make it a very attractive choice for higher power applications. Each of the three current sensors that were investigated appear to provide satisfactory performance, but further work needs to be done to gain a better understanding of their transient behavior.

VI. REFERENCES

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